'80 SEMICONDUCTOR DATA BOOK

HITACHI IC MEMORIES

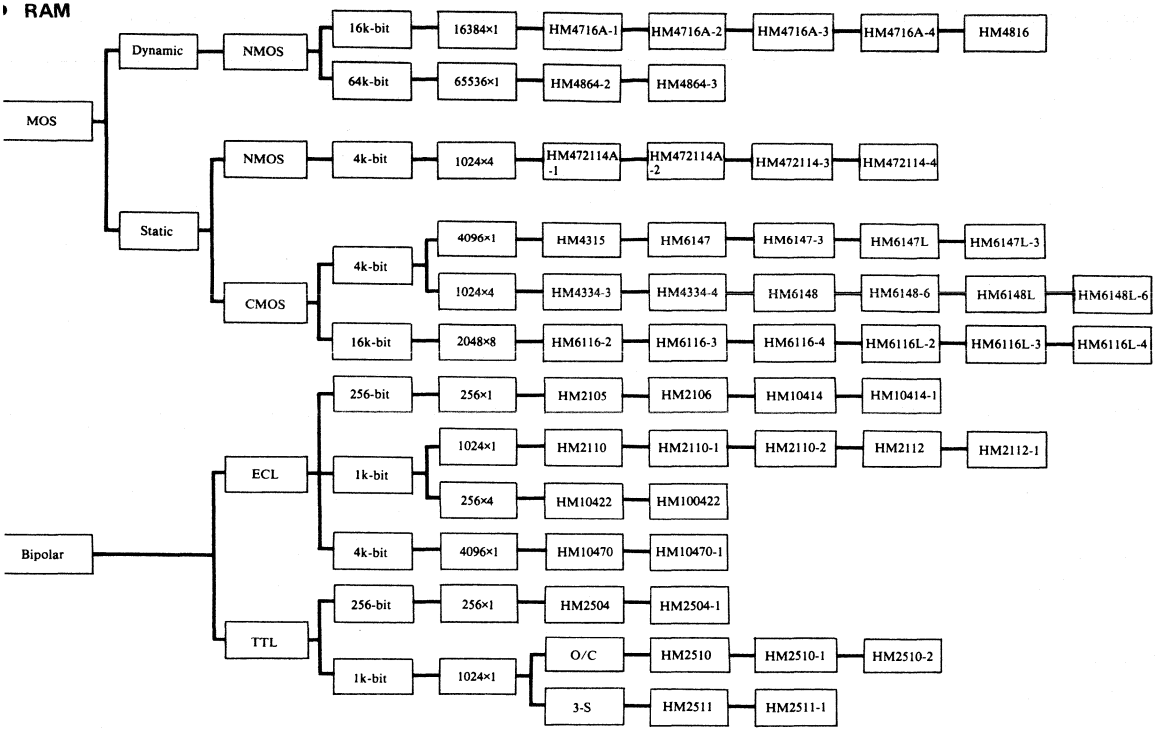
INDEX

NOTICE

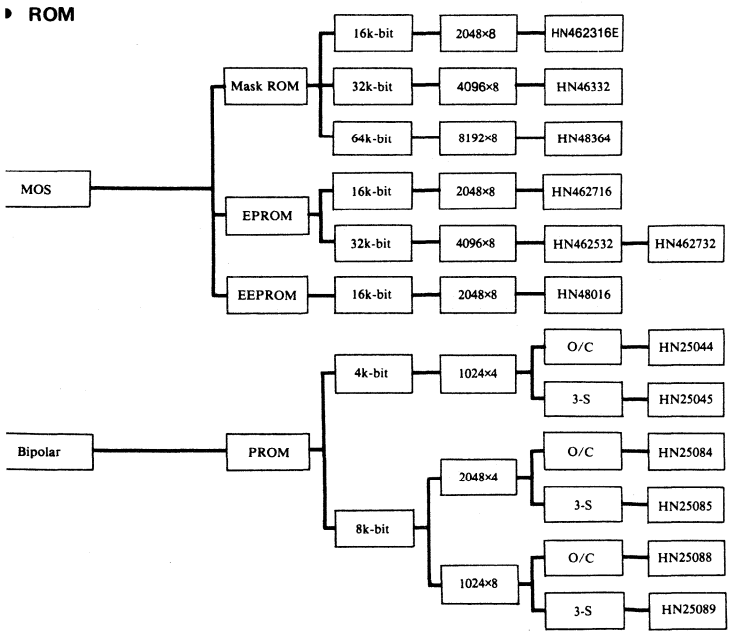
The example of an applied circuit or combination with other equipment shown herein indicates characteristics and performance of a semiconductor-applied product.
The Company shall assume no responsibility for any problem involving a patent caused when applying the descriptions in the example.

■ CURRENT LINE OF HITACHI IC MEMORIES

▸ RAM



▸ ROM



■ TYPICAL CHARACTERISTICS OF RANDOM ACCESS MEMORIE

• MOS RAM

Type No.	Process	Number of bit	Organization	Mode	Access Time (ns)max.	Cycle Time (ns)min.	Supply Voltage (V)	Power Dissipation (mW)	Package*				Replacement
									Pin No.	C	G	P	
HM472114A-1	NMOS	4K	1024 × 4	Static	150	150	+5	200	18		○	○	
HM472114A-2					200	200					○	○	Intel 2114L-2
HM472114-3					300	300	+5	200	18		○	○	Intel 2114L-3
HM472114-4					450	450					○	○	Intel 2114L
HM4334-3	CMOS				300	460	+5	20	18			○	Harris HM-6514
HM4334-4					450	640						○	
HM6148					70	70	+5	200	18			○	Intel 2148
HM6148-6					85	85						○	Intel 2148-6
HM6148L					70	70	+5	200	18			○	
HM6148L-6					85	85						○	
HM4315			4096 × 1		450	640	+5	20	18			○	
HM6147					70	70	+5	75	18		○	○	Intel 2147
HM6147-3					55	55					○	○	Intel 2147-3
HM6147L					70	70	+5					○	
HM6147L-3					55	55						○	
HM6116-2		16K	2048 × 8		120	120	+5	180	24			○	
HM6116-3					150	150						○	
HM6116-4					200	200						○	
HM6116L-2					120	120	+5	160	24			○	
HM6116L-3					150	150						○	
HM6116L-4					200	200						○	
HM4716A-1	NMOS	16K	16384 × 1	Dynamic	120	320	+12, +5, −5	350	16		○	○	
HM4716A-2					150	320					○	○	Mostek MK4116-2
HM4716A-3					200	375					○	○	Mostek MK4116-3
HM4716A-4					250	410					○	○	Mostek MK4116-4
HM4816					100	200	+5	250	16	○			
HM4864-2†		64K	65536 × 1		150	270	+5	170	16	○			
HM4864-3†					200	335				○			

• Bipolar RAM

Type No.	Level	Number of bit	Organization	Output	Access Time (ns)max.	Supply Voltage (V)	Power Dissipation (mW/bit)	Package*				Replacement
								Pin No.	C	G	P	
HM2105	ECL	256	256 × 1	Open Emitter	35	−5.2	1.8	16		○		Fairchild F10410
HM2106					15		1.8	16		○		
HM10414†					10		2.8	16		○		Fairchild F10414
HM10414-1†					8		2.8	16		○		
HM10422†		1K	256 × 4		10		0.8	24		○		Fairchild F10422
HM100422†					10	−4.5	0.8	24		○		Fairchild F100422
HM2110			1024 × 1		35	−5.2	0.5	16		○		Fairchild F10415A
HM2110-1					25		0.5	16		○		
HM2110-2					20		0.5	16		○		
HM2112					10		0.8	16		○		
HM2112-1					8		0.8	16		○		
HM10470†		4K	4096 × 1		25		0.2	18		○		Fairchild F10470
HM10470-1†					15		0.2	18		○		
HM2504	TTL	256	256 × 1	Open Collector	55	+5.0	1.8	16		○		Fairchild 93411
HM2504-1					45		1.8	16		○		Fairchild 93411A
HM2510		1K	1024 × 1		70		0.5	16		○		
HM2510-1					45		0.5	16		○		Fairchild 93415
HM2510-2					35		0.5	16		○		Fairchild 93415A
HM2511				3-state	70		0.5	16		○		
HM2511-1					45		0.5	16		○		Fairchild 93425

*: The package codes of C, G, and P are applied to the package materials as follows.
C; ceramic with Lid, G; Glass-Sealed Ceramic, P; Plastic.
†: Preliminary.

■ TYPICAL CHARACTERISTICS OF READ ONLY MEMORIES

• MOS ROM

Type No.	Program	Number of bit	Organization	Process	Access Time (ns) max.	Supply Voltage (V)	Power Dissipation (mW)	Package*				Replacement
								Pin.No.	C	G	P	
HN462316E	Mask	16K	2048 × 8	NMOS	350	+5	350	24			○	Intel 2316E
HN46332		32K	4096 × 8		350		250	24			○	Mostek MK32000
HN48364		64K	8192 × 8		350		225	24			○	Mostek MK36000
HN462716	UV Erasable and Electrically Programmable	16K	2048 × 8		450		310	24	○	○		Intel 2716
HN462532		32K	4096 × 8		450		450	24	○			Texas TMS2532
HN462732								24	○			Intel 2732
HN48016	Electrically Erasable and Programmable	16K	2048 × 8		350		160	24			○	

• Bipolar PROM

Type No.	Number of bit	Organization	Output	Access Time (ns) max.	Supply Voltage (V)	Power Dissipation (mW)	Package*				Replacement
							Pin No.	C	G	P	
HN25044	4K	1024 × 4	Open Collector	50	+5	500	18		○		Signetics 82S136
HN25045			3-state						○		Signetics 82S137
HN25084†	8K	2048 × 4	Open Collector	60		600	18		○		Signetics 82S184
HN25085†			3-state						○		Signetics 82S185
HN25088†		1024 × 8	Open Collector	60		600	24		○		Signetics 82S180
HN25089†			3-state						○		Signetics 82S181

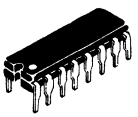
*: The package codes of C, G, and P are applied to the package materials as follows.
C: Ceramic with Lid, G: Glass-sealed ceramic, P: Plastic.
†: Preliminary.

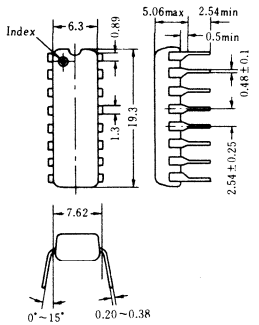
■ PACKAGING INFORMATION (Dimensions in mm)

Hitachi IC Memories are classified into 3 types; dual-in-line plastic type, dual-in-line ceramic (glass-sealed) type and dual-in-line ceramic (with lid) type, according to the quality of material used for packaging.
Therefore, after taking into consideration the operation environment and other conditions, please select the optimum packaging. Moreover, it is requested that the packaging material quality code be specified when orders are placed for types having a plural packaging material quality in the same variety.

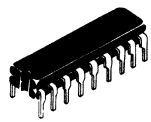
● DUAL-IN-LINE PLASTIC

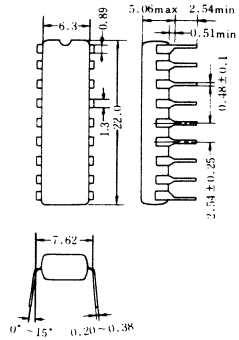
● DP-16



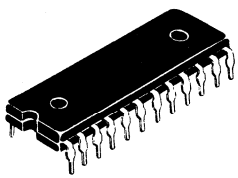


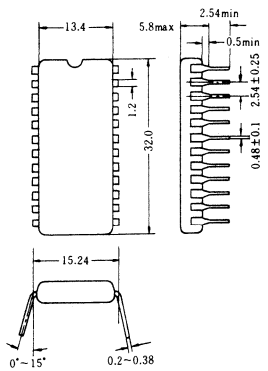
● DP-18





● DP-24



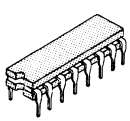


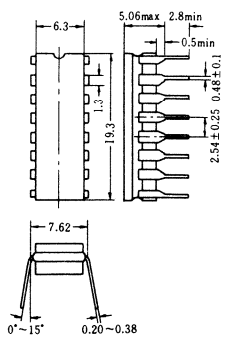
Applicable ICs

DP-16	HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4,
DP-18	HM472114AP-1, HM472114AP-2, HM472114P-3, HM472114P-4, HM4334P-3, HM4334P-4, HM6148P, HM6148P-6, HM6148LP, HM6148LP-6, HM4315P, HM6147P, HM6147P-3, HM6147LP, HM6147LP-3
DP-24	HM6116P-2, HM6116P-3, HM6116P-4, HM6116LP-2, HM6116LP-3, HM6116LP-4, HN462316EP, HN46332P, HN48364P, HN48016P

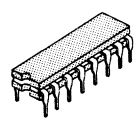
● DUAL-IN-LINE CERAMIC (Glass-sealed)

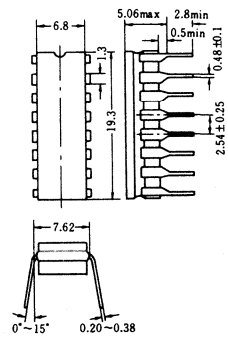
● DG-16





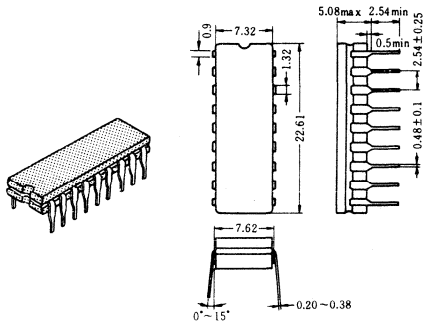
● DG-16A



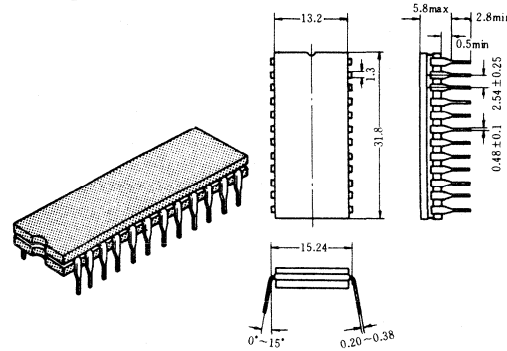


HITACHI

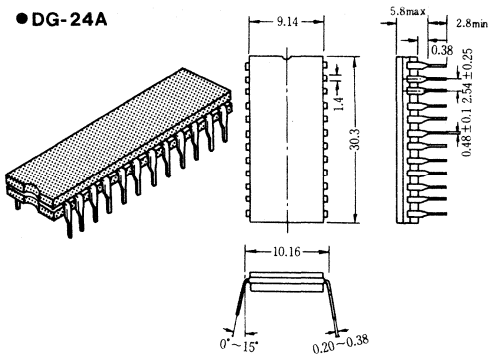
● DG-18



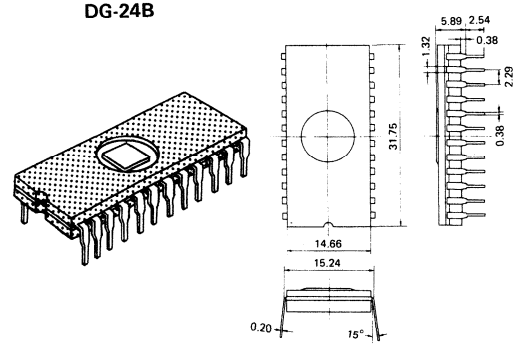
● DG-24



● DG-24A



DG-24B



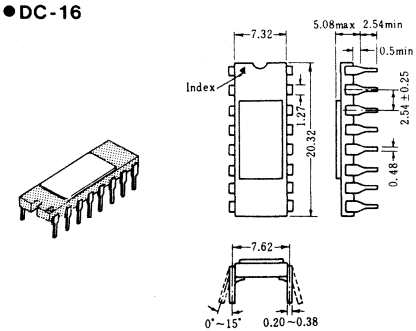
Applicable ICs

DG-16	HM2105, HM2106, HM10414, HM10414-1 HM2504, HM2504-1, HD2912
DG-16A	HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4, HM2110, HM2110-1, HM2110-2, HM2112, HM2112-1, HM2510, HM2510-1, HM2510-2, HM2511, HM2511-1, HD2916, HD2923

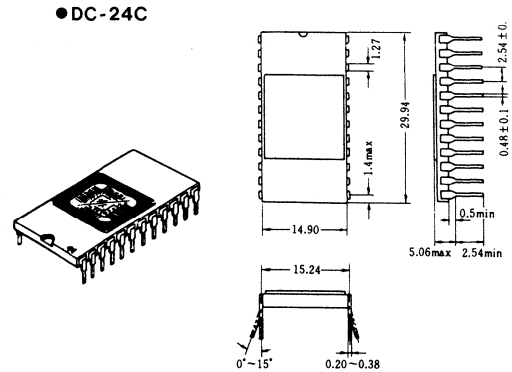
DG-18	HM72114A-1, HM472114A-2, HM472114-3 HM472114-4, HM10470, HM10470-1, HN25044, HN25045, HN25084, HN25085
DG-24	HN25088, HN25089
DG-24A	HM10422, HM100422
DG-24B	HN462716G

DUAL-IN-LINE CERAMIC (with Lid)

● DC-16



● DC-24C



Applicable ICs

DC-16	HM4816, HM4864-2, HM4864-3
DC-24C	HN462716, HN462532, HN462732

■ RELIABILITY OF HITACHI IC MEMORIES

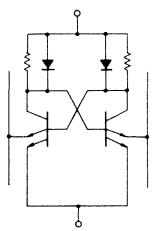
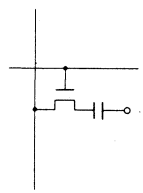
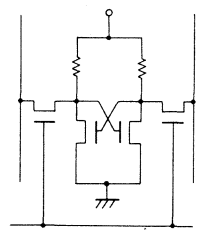
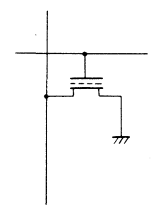
1. Structure

There are Bipolar type and MOS type IC memories. The former has a characteristic of an extremely high speed. But it is a comparatively small capacity and on the other hand, latter features a large capacity. These IC memories are utilized by effectively taking the most of their respective characteristics.

Flows from designing, manufacturing and up to inspection for both Bipolar and MOS type IC memories are established under a unified concept, design and inspection standards. Therefore stable results concerning their reliability have been obtained with these IC memories, regardless of differences in the circuit design, pattern, layout, degree of integration, etc.

From its characteristics, the memory LSI is integrated in high density by unit patterns called "cell" and it is not exaggeration to say that they are produced in the most advanced semiconductor manufacturing technologies. To get the high reliability of such a memory which has been subjected to rapid technological advances, know-hows based on past experience from the design stage of a cell are incorporated. Farther to evaluate reliability of each respective technology applied. Reliability evaluation using TEG (Test Element Group), etc. is carried out. Examples of cell circuits of the Bipolar memory and MOS memory are shown in Table 1.

Table 1 Examples of Basic Cell Circuit of IC Memories

Classification	Bipolar memory	NMOS memory (Dynamic RAM)	NMOS, CMOS memories (Static RAM)	NMOS memory (PROM)
Application	Buffer memory, control memory of high-speed computer	Main memory of computer, microcomputer memory		For microcomputer control
Example of basic cell circuit				

2. Reliability data

Results of reliability tests are listed below.

(1) Example of failure criteria

Failure criteria for the Bipolar type are the same as the criteria for TTL and ones for MOS are the same as the MOS LSI failure criteria. Some of the MOS type dynamic memories require 3 types of power souces V_{DD}, V_{BB}, and V_{CC}. However, since an operating range of ±10% is independently guaranteed for each of the power sources, electrical inspection in the function test and others, is carried out under all respective combinations.

(2) Reliability test data on Bipolar memories

The reliability test data on the Bipolar memories are shown in Tables 2 and 3. Since they are manufactured under the aforementioned standardized design rules and quality control, there is no difference in reliability among various types. In addition, it can be said that the greater the capacity, the higher the reliability per bit.

(3) Reliability test data on MOS memories

The reliability test data on the MOS memories are shown in Tables 4, 5 and 6. In these tables, data are shown on representative types of HM4716A (16K bit dynamic), HN462716 (16K bit PROM), HM472114P (4K bit static) and HM6147P (4K bit static).

Table 2 Results on Bipolar Memories of Reliability Tests (1)

Test item	Test condition	HM2504 Ceramic (Metal-lid)				HM2510 Ceramic (Glass-sealed)			
		Samples	Total component hours	Failures	Failure rate*	Samples	Total component hours	Failures	Failure rate*
High temperature (DC bias)	Ta = 125°C V_{CC} = 5.25V	125	C.H. 2.3×10^{5}	0	1/hr 4.1×10^{-6}	75	C.H 1.6×10^{5}	0	1/hr 5.7×10^{-6}
	Ta = 150°C V_{CC} = 5.25V	75	1.3×10^{5}	0	6.9×10^{-6}	40	0.7×10^{5}	0	1.3×10^{-5}
	Ta = 175°C V_{CC} = 5.25V	30	0.5×10^{5}	0	1.7×10^{-5}	40	0.7×10^{5}	0	1.3×10^{-5}
High temperature (Dynamic operation)	Ta = 125°C V_{CC} = 5.25V t_{cyc} = 10μs	–	–	–	–	300	6.0×10^{6}	0	1.5×10^{-7}
ON/OFF bias	Ta = 25°C V_{CC} = 5V ON: 3 minutes, OFF: 3 minutes,	50	cycles 11,000	0	–	30	cycles 8,500	0	–
High-temperature storage	Ta = 200°C	30	0.8×10^{5}	0	1.2×10^{-5}	20	0.4×10^{5}	0	2.3×10^{-5}
	Ta = 259°C	20	0.5×10^{5}	0	1.8×10^{-5}	20	0.6×10^{5}	0	1.5×10^{-5}
	Ta = 295°C	30	0.8×10^{5}	1	2.7×10^{-5}	10	0.3×10^{5}	1	6.7×10^{-5}
Temperature cycling	−55°C ~ 150°C 3 cycles/hour	50	cycles 3,500	0	–	30	cycles 1,000	0	–

* Estimated failure rate with confidence level 60%.

Table 3 Results on Bipolar Memories of Reliability Tests (2)

Test item	Test condition	HM2504 Ceramic (Metal-lid)		HM2510 Ceramic (Glass-sealed)	
		Samples	Failures	Samples	Failures
Temperature cycling	−65°C ~ 150°C 10 cycles	22	0	22	0
Soldering heat	260°C 10 seconds	22	0	22	0
Thermal shock	0°C ~ 100°C 10 cycles	22	0	22	0
Mechanical Shock	1,500G, 0.5ms Three times each for X, Y, and Z	22	0	22	0
Variable frequency	100 ~ 2,000Hz, 20G reciprocation 4 minutes Three times each for X, Y and Z	22	0	22	0
Constant-accelaration	20,000G 1 minute each for X, Y and Z	22	0	22	0

Table 4 Results on MOS Memories of Reliability Tests (1)

Test item	Test condition	HM4716A Ceramic (Glass-sealed)				HN462716 Ceramic (glass lid)				Remarks
		Samples	Total component hours	Failures	Failure rate*	Samples	Total component hours	Failures	Failure rate*	
High-temperature dynamic operation	Ta = 125°C V_{CC} = 13.2V, t_{cyc} = 10μs; HM4716A V_{CC} 5.5V, t_{cyc} = 5μs; HN462716	831	C.H. 1.04×10^{6}	1*1	1/hr 1.94×10^{-6}	48	C.H. 5.1×10^{2}	0	1/hr 1.89×10^{-5}	*1 Defective oxide
High-temperature storage	Ta = 200°C	10	2.0×10^{4}	0	4.6×10^{-5}	40	6.0×10	0	1.5×10^{-5}	
High-temperature storage	Ta = 259°C	10	2.0×10^{4}	0	4.6×10^{-5}	38	5.7×10^{4}	4*2	9.2×10^{-5}	*2 Data disappearance × 4
High-temperature storage	Ta = 295°C	30	6.0×10^{4}	0	1.5×10^{-5}	40	6.0×10^{4}	7*3	1.4×10^{-4}	*3 Data disappearance × 7
High-temperature and high-humidity storage	Ta = 80°C RH = 90%	20	4.0×10^{4}	0	2.3×10^{-5}	10	1.0×10^{4}	0	9.2×10^{-5}	
Low-temperature storage	Ta = −65°C	20	4.0×10^{4}	0	2.3×10^{-5}	22	2.2×10^{4}	0	4.2×10^{-5}	

* Estimated failure rate with confidence level 60%.

Table 5 Results on MOS Memories of Reliability Tests (2)

Test item	Test condition	HM472114P				HM6147P				Remarks
		Samples	Total component hours	Failures	Failure rate*	Samples	Total component hours	Failures	Failure rate*	
High-temperature pulse Actuation	Ta = 125°C V_{CC} = 5.5V, t_{cyc}= 10μs	60	C.H. 1.2×10^5	0	1/hr 7.7×10^{-6}	196	C.H. 1.96×10^5	0	1/hr 4.7×10^{-6}	
High-temperature storage	Ta = 150°C	30	6.0×10^4	0	1.5×10^{-5}	20	2.0×10^4	0	4.6×10^{-5}	
High-temperature and high-humidity storage	Ta = 65°C RH = 95%	551	9.1×10^5	1*1	2.2×10^{-6}	–	–	–	–	*1 Aluminum corrosion
High-temperature and high-humidity storage	Ta = 80°C RH = 90°C	–	–	–	–	20	2.0×10^4	0	4.6×10^{-5}	
High-temperature and high-humidity bias	Ta = 85°C, RH = 85% V_{CC} = 5.5V, HM472114P V_{CC} = $\overline{CS}$ = 7V, HM6147P	340	5.8×10^5	0	1.6×10^{-6}	20	4.0×10^4	0	2.3×10^{-5}	

* Estimated failure rate with confidence level 60%.

Table 6 Results on MOS Memories of Reliability Tests (3)

Test item	Test condition	HM4716A		HN462716		HM472114P		HM6147P		Remarks
		Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	
Temperature cycling	–65°C ~ 150°C 10 cycles	750	0	25	0	–	–	–	–	
Temperature cycling	–55°C ~ 150°C 10 cycles	–	–	–	–	1,392	0	38	0	
Thermal shock	0°C ~ 100°C 10 cycles	38	0	25	0	20	0	20	0	
Soldering heat	260°C, 10 seconds	38	0	25	0	20	0	18	0	
Mechanical Shock	1,500G, 0.5ms Three times each for X, Y and Z	38	0	25	0	22	0	–	–	
Variable frequency	100 ~ 2,000Hz, 20G Reciprocation 4 minutes Three times each for X, Y and Z	38	0	25	0	22	0	–	–	
Constant-acceleration	20,000G 1 minute each for X, Y and Z	38	0	–	–	22	0	–	–	

(4) Change of electrical characteristics under endurance test for IC memories

The degradation of I_{CBO} of the cell transistor, degradation of h_{FE}, etc., can be considered as main factors in the internal elements for reliability of Bipolar memories. In actual element designing, however, it has been designed to operate in the range at which these degradations do not happen. Therefore changes of electrical characteristics including access time are not observed. A example of change in the access time is shown in Table 7.

V_{TH} is a basic parameter in the MOS memories; however, it has been confirmed there is not any shift in V_{TH} for practical usage because we have applied surface stabilizing technique, clean process, etc. The change of V_{BB} min which is one of the detective parameters for degradation of V_{TH} in case of MOS memories is shown in Table 8.

(5) Classification of failure modes

Examples of failures happened in the field are shown in Figs. 1 and 2. Since memory LSIs generally require the most fine processing in semiconductor manufacturing technology, the percentage of failures resulting from pinholes, photoresist defects, foreign materials, etc., is tending to increase. To eliminate the latent defects which are generated in these manufacturing processes, we are constantly improving these processes, and performing burn-in screening under high temperature for all memories. In addition, since the analysis of failures in the field can result in important feedback to improve their design and manufacturing, we are always exerting our efforts to collect field data with the aim of further establishing their high reliability.

Table 7 Example of Change in Bipolar Memory Characteristics

Example	
Nomenclature	HM2510
Test condition	Ta = 125°C, V_{CC} = 5.5V
Failure criteria	t_{AA} = 70ns
Failure mechanism	Surface degradation

Results:
Access time (t_{AA}) is stabilized and is within the failure criteria.

Example of time change in access time for Bipolar memory

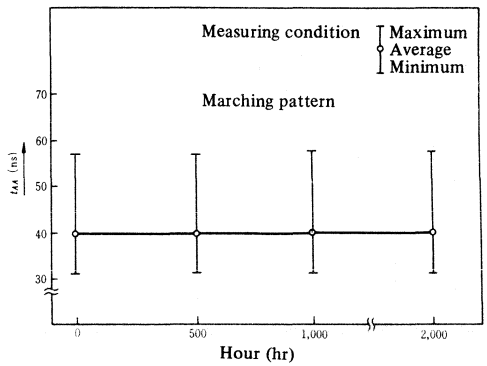


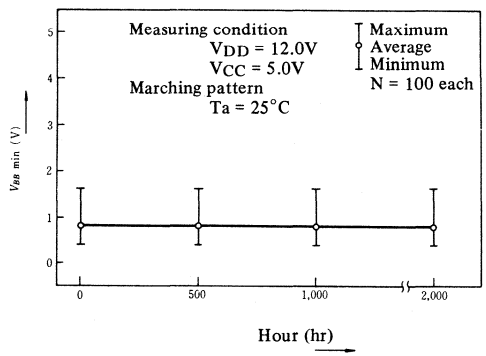
Table 8 Example of Change in MOS Memory Characteristics

Example	
Nomenclature	HM4716A
Test condition	Ta = 125°C, V_{DD} = 13.2V Dynamic operation
Failure criteria	$\|V_{BB}\|$ = 4.5V or ΔV_{BB} = 1.0V
Failure mechanism	Surface degradation

Results: There is no degradation in the power voltage margin and it is stabilized.

Remarks: Measuring accuracy is ±0.2V.

Example of time change in V_{BB}min.



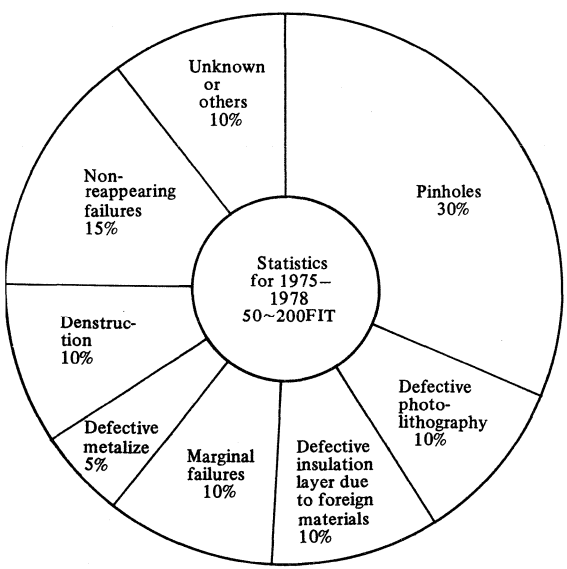


Fig. 1 Classification of Failure Modes of MOS Memory in the field

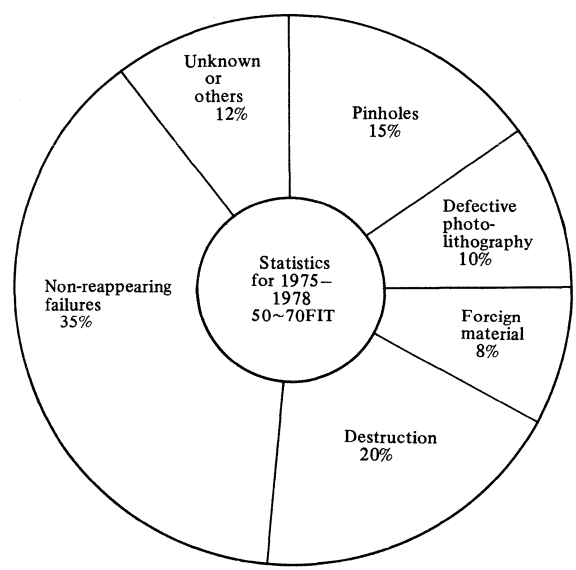
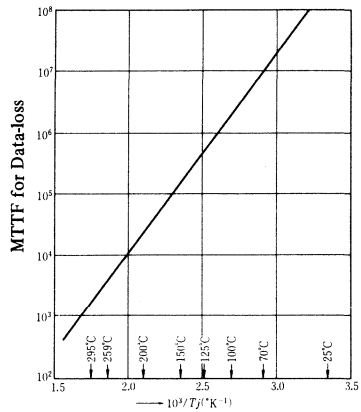


Fig. 2 Classification of Failure Modes of Bipolar Memory in the field

(6) Failure rate and derating

An example of PROM derating curve for EPROM is shown in Table 9. Generally, since the recommended operating conditon of the IC memory is fixed, it is common to take into account only temperature when the user performs derating. However, since lowering its junction temperature in usage is expected to provide a more stabilized operation from the aspects of access time or refresh time and other characteristics, we would like you to take into account this effect.

Table 9 Example of Derating Characteristics on HN462716

Example		Derating curve of MOS EPROM HN462716
Stress factor	Temperature	
Failure criteria	Electrical characteristics, function test	
Failure mechanism	Data-loss	
Summary: The derating curve on the right has been obtained under high-temperature storage test for EPROM HN462716.		
Remarks		How to use a derating data High reliability can be expected from the decrease of junction temperature in the above figure. The junction temperature is obtained from equation $Tj = Ta + \theta ja \cdot Pd$ · Whereas, θja is the thermal resistance of the package, which is about 100°C/W in windless condition and about 60 ~ 70°C/W at the wind velocity of 2.5 m/s.

■ PRECAUTIONS FOR HANDLING IC MEMORIES

A variety of IC memories of high-speed, high-power and static low power dissipation CMOS have been developed and commercially available, which allows an electronics designer to properly select the one best suited for a particular application. However, he must be familiar with the advantages and disadvantages of the devices to make the optimum selection and to prevent them from malfunctioning or, in the worst case, from breaking down. Precautions for handling IC memories given below will help the electronics designers to work out their optimum circuit designs.

1. Bipolar IC Memory

1.1 Prevention of static electricity

Bipolar ICs have been considered to have higher resistance to the static electricity than MOS ICs. However, the presently availabe high speed IC, represented by bipolar memories, must be provided with a suitable preventive measure against the static electricity. Because their diffused junctions have become thinner than the conventional types, in order to perform higher capability. Take note of the following points.

(1) Keep all terminals of a device in the conductive mat during transportation and storage to keep them at the same potential. A conductive mat called "MOSPAK" is commercially available. Unless otherwise specially stated, all HITACHI IC memories will be shipped in our conductive mats. Store them as they are.

(2) When handling by hand IC memories for inspection or connection, his finger must be grounded as shown in Fig. 1. Do not forget to insert a 1M ohm resistor to protect him against an electric shock.

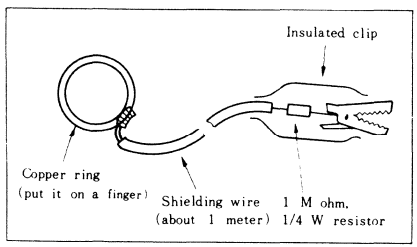


Fig. 1 An example of human body grounding

(3) It is advisable to control the ambient relative humidity at about 50 per cent to prevent the occurrence of static electricity.

(4) It is also recommendable to wear cotton clothes instead of the ones made of synthetic fabrics to prevent the static electricity from occurring.

(5) It is desirable to ground the soldering iron tips. Use a low voltage soldering iron (12 or 24V), if possible.

(6) When IC memories mounted on the circuit boards are shipped, it is preferable to pack them with conductive mats.

1.2 Cooling down

A bipolar memory will dissipate about 0.5 W of power notwithstanding it is operated or not operated. For instance, a 1K byte memory card consisting of 36 peices of HM2510 devices will dissipate about 20 Watts. Since the heat generated by such a circuit board is too great to be removed by the natural convection, a forced air cooling system having a capability of 2.5 m/s or more air blow must be installed. A large memory system must be installed in a sealed housing which has a pair of air inlet and outlet.

1.3 Preventive measures for reverse insertion

If a device is reversely connected, an excessive current will flow to burn the connection leads to the memory chip resulting in breakdown of the device, because its V_{CC} and ground terminals are symmetically positioned. Locate the pin No. 1 which is indicated by a mark on the top surface of each device and provide the device with correct connection.

2. MOS IC Memory

2.1 Prevention of static electricity

Similar to bipolar IC memories, suitable preventive measures should be taken for MOS IC memories by referring to paragraph 1.1.

2.2 Absorption of power source noise

The source current level flowing in the dynamic memory during the time of access is considerably different from that of stand by. Although the current difference is quite effective to save the power consumption, the current spike may be developed into the power source noise. Since all MOS IC memories are, in general, accessed while being refreshed, it is recommended to insert large capacitors (a 10 μF capacitor for every 9 pieces of 16K-bit HM4716A, for example) as well as a 0.1 μF capacitor having good high-frequency characteristics for each memory. Needless to say, it is very important to reduce the power circuit impedance when designing.

2.3 Current spike in V_{BB} power

The V_{BB} power is necessary for maintaining the IC memory function in the reverse bias and the current does not generally exceed the level of the reverse leakage current. However, in order to prevent an accidental current spike which is sharply formed in either positive or negative phase by the rise or fall clock pulse at the time of access, use a 0.1 μF capacitor for every 2 or 3 memories for absorbing such noises.

2.4 Clock driver ICs

The TTL to MOS clock driver ICs have special designs so that they are capable of quick increase in the capacitive load. If a ground wire short-circuits either V_{DD} or V_{CC}, which appear in the Pin No. 1 and No. 16 respectively, when the device is at high level, the device may be broken down. Carefully eliminate such possibility beforehand.

2.5 Power application sequence

It is advisable to design the circuits so that power is applied in the sequence of V_{BB}, V_{DD} and V_{CC} and interrupted in the reverse sequence, here the reverse bias V_{BB} is applied first and interrupted last.

It may be impossible for some small-scaled systems to apply power in the above-mentioned sequence (for example, when the V_{BB} is supplied by a DC to DC converter). According to our experiments conducted in the under-mentioned test conditions, it has been proved that such a small-scaled system as to consist of 200 to 300 memory devices is not affected by the power application sequence.

Power application sequence test for N MOS IC

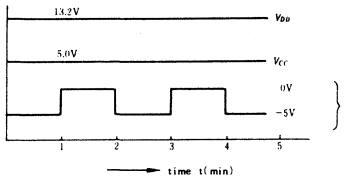
1.) Test method

(1) Ambient temperature: 25°C

(2) Power voltage: V_{DD}=13.2V, V_{CC}=5.0V, V_{IH}=5.0V

(3) Operation mode: AC operation ("0" to "16383" all bits scanning). t_{cyc}= 10 μs Read modify write operation

(4) V_{BB} power: ON (1 min.) – Floating (1 min.)



2.) Test results

Type No.	Number of cycles	Number of samples	Number of failures
HM4716A	2000 cycles	50	0

2.6 Assessment of the memory system design

It is quite effective to obtain the power margin curves (shmoo curve) for evaluating the memory system designs (timing margin or adaptability to the peripheral circuits). Investigate the V_{BB} and V_{DD} power behaviors by gradually varying their levels, and the ones which are closer to the margine shown by the memory device itself can be judged to be better than others.

2.7 Overhead parity bit

Application of MOS IC static memory especially to micro-computers has been rapidly increasing due to the advantages that MOS static memory is operated by a single 5V power source and refreshing is not required.

There are some cases where all bits are used as the information bit without inclusion of any parity bit by some circuit designing reasons. It is, however, desirable to add parity bits to thoroughly avoid the memory error.

■ OUTLINE OF TESTING METHOD

. Inspection Method

ɔmpared to conventional core memories, all peripheral rcuits such as the decoder circuit, write circuit, read circuit, :c., are contained within the IC memories. As a result, all orks of assembling the parts and performing electrical inspec-on, which had been carried out by core memory manufac-ırers in the past, have be come to be incorporated as works of ɔ manufacturers. Consequently, the electrical inspection of ıe memory IC has been faced to a more systematic inspection ıethod and conventional IC inspection facilities have become ɔmpletely useless. This has led to the development and intro-ıuction of a memory tester with pattern generator to generate ıe inspection pattern of the memory IC at high speed. A ınction test for such as TTL gates can be performed even by comparatively simple DC parameter facility. However, when ıe address input becomes multiplexed as in 16K memory, ven the generation of the function test pattern becomes a ɛrious problem. In the memory IC inspection, its quality annot be judged by only inspecting DC characteristics related ɔ external pins. This is because numbers of transistors, etc., ɛlated to the DC characteristics of the pins only amount to /1000 of all element numbers within IC memories. The ɔllowing various address patterns are proposed to inspect 'hether or not the internal circuits are functioning correctly.

1) All "Low", all "High"
2) Checker flag
3) Stripe pattern
4) Marching
5) Galloping
6) Walking
7) Ping-pong

ılthough there are a lot of address patterns, only representative nes have been listed. These patterns are convenient for hecking the mutual finterference of bits and sometimes are atterns with maximum power dissipation. Among the above-ıentioned patterns, those of (1) to (4) are the socalled N atterns and these patterns are capable of checking IC memo-ies of N bits with several sequences of N at most against the ıemory IC of N bits. Whereas, those of (5) to (7) are called I^2 patterns and they need patterns several sequences of N^2.

ı serious problem arises in using the N^2 patterns in a large-apacity memory, For example, a long period of about 30 ıinutes becomes necessary to perform inspection of the 16K ıemory with galloping pattern. Patterns from (1) to (3) are omparatively simple and good methods, but they are not ıerfect against a failure in the decoder circuit. As the most imple pattern for inspecting the necessary memory function, here is a "Marching" pattern.

2. Marching Pattern

The marching pattern, as its name indicates, is a pattern in which "1"s march into all bits written in "0"s. The addressing method will be explained for a simple 16 bit memory as an example.

(1) Write "0" for all bits . . . . . Fig. 1(a)
(2) Read "0" of 0th address and check that the read data is "0". Hereafter, the meaning of "Read" is "checking and judging the data".
(3) Write "1" in the 0th address . . . . . Fig. 1 (b)
(4) Read "0" of 1st address
(5) Write "1" in 1st address
(6) Read "0" of nth address
(7) Write "1" in nth address . . . . . Fig. 1 (c)
(8) Repeat above procedures (6) and (7) up to the last. Finally, all data will become "1".
(9) Since all data are "1"s in this condition, replace "0" and "1" after procedure (2) and repeat once more up to procedure (8).

It is understood that 5N address patterns are necessary for the N bit memory in this method.

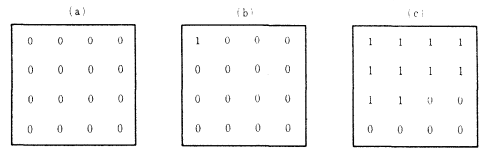


Fig. 1 Addressing method for 16 bits memory in the Marching pattern

3. Generation of Marching Pattern

The method of generating the marching pattern and displaying failed bits of the memory on the Braun tube will be introduced. Fig. 2 shows the all block diagram. The address pattern is generated by using four synchronous 4 bit counters. All address patterns are shown in Fig. 4. This example, is for 16K bit memory, however, it can be easily understood that A14 which has a half frequency of the maximum address input A13 is the same as the data input.

The A15 signal together with the carrier signal of HD74161 is used to determine the termination of the sequence.

As shown in Fig 2. In the read and write cycles after cleaning all bits addressing is twice the period of clearing. This switching is performed at the gate of the binary circuit following the reference pulse generating circuit.

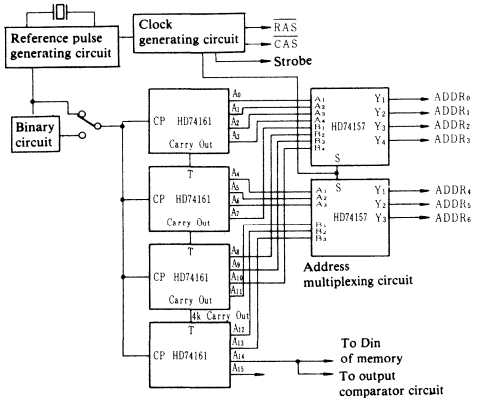


Fig. 2 Marching Pattern Generating Circuit

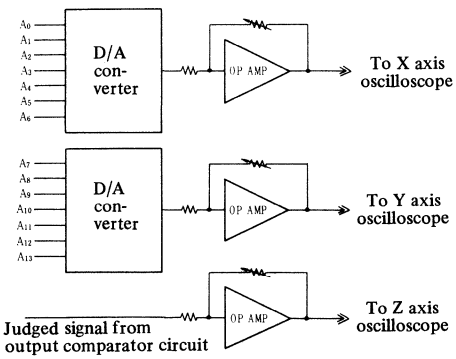


Fig. 3 Fail Bit Map Display Circuit

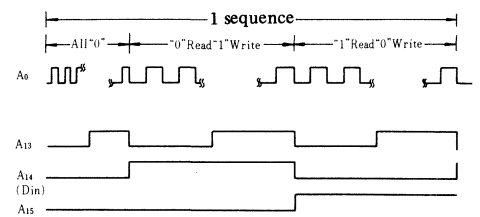
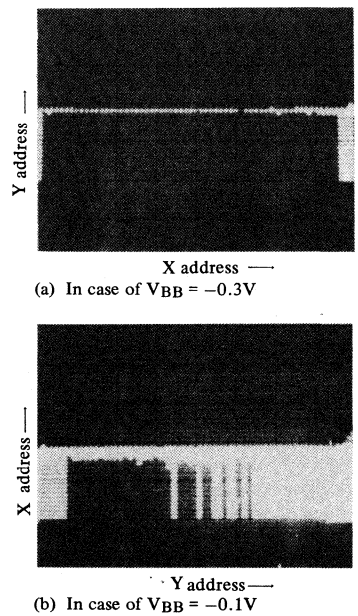


Fig. 4 Entire Pulse Relations

Input the output of HD74161 is input to the D/A converter and the output of D/A converter is connected to the oscilloscope to display → X-Y matrix. The output of the comparator circuit is connected to the Z axis and performs luminous intensity modulation. In this way, the fail bit map can be displayed on the CRT. Fig. 5 shows an example checking a voltage margin. By changing the power voltage V_{BB}, the increase and decrease of the failed bits can be well understood. The operation of the memory can be dynamically understood by displaying its operation on the CRT. The operation of the memory IC is extremely complicated differing from other TTLs, etc.. Its operation is not easy to understand by pulse waveform observation with an ordinary oscilloscope. The fail bit map as shown in Fig. 5 is extremely useful. It is capable of visually understanding the operation of memory IC.



(a) In case of $V_{BB} = -0.3V$

(b) In case of $V_{BB} = -0.1V$

Fig. 5 Example of Dependency of Fail Bit Map on V_{BB}

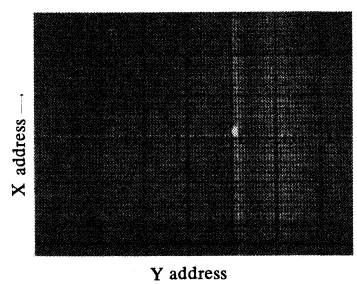


Fig. 6 Example of 1 bit solid fail

4. Failure Mode

Generally, failure 70% ~ 90% of failures at users are of those called solid failure. This failure mode has no relation with access time, voltage margin and timing, and is not capable of reading from or writing to certain specified bits and is failure fixed to "0" or "1". An example of a single bit solid failure is shown in Fig. 6. The convenient checker, previously mentioned as simple tester, is sufficiently capable of detecting such failures. Therefore, with the exception of special cases, it can be considered that the necessity of performing high-precision measurements such as those made by memory IC manufacturers is rare.

In the inspection of memory IC at out company, full inspection under the worst conditions are performed so as to guarantee sufficient operations under all power voltage conditions and timing conditions listed in the data sheet.

An extremely accurate memory tester becomes necessary for performing high-precision inspeciton with 1ns accuracy. Our company is developing IC memory testers to supply memory ICs with excellent characteristics and quality to users and is establishing the system capable of developing further high-efficiency memory ICs.

1. Programming & Erasing of EPROM HN462716

1.1 Programming

Programming to the memory cell of HN462716 is achieved by applying a high voltage to the drain and gate. The high voltage of the drain raises the electron energy of the channel and the voltage of the gate induces the high energy electron (hot electron) injecting to the floating gate. Thus, the charge injected to the floating gate changes the threshold voltage of the memory cell and stores it as the memory information gate changes the threshold voltage of the memory cell and stores it as the memory information.

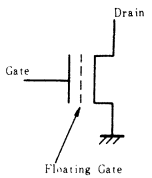


Fig. 1 Equivalent circuit shematic of memory cell

Initially, and after each erasure all bits of the HN462716 are in the "1" state. The HN462716 is in the programming made when the V_{PP} power supply is at 25 V and $\overline{OE}$ is at V_{IH}.
Data can be programmed ("1" → "0") by applying the timing relation waveform stipulated in the specification of HN462716. Programming can be made to a sequential address and a random address. In addition, writing of only 1 word is also possible. Bits programmed in this manner become "0" in normal power supply condition, however, the output data inverses to "1" when V_{CC} is rises. This voltage (READ V_{CC}) becomes the index for confirming how sufficiently programming has been made to the floating gate. (Of course, the switching speed, input/output levels and others cannot be guaranteed in the range exceeding the power supply condition of V_{CC}.) Fig. 2 shown the correlations among this READ V_{CC}, program pulse width (t_{PW}) and V_{PP} voltage and it indicates the characteristics of a standard type memory cell.
It can be understood from Fig. 2 that the higher the V_{PP} and wider the t_{PW}. the more sufficient is the programming. However, there lies a possibility of breakage of the cell when the V_{PP} becomes too high and exceeds the withstand voltage of the device. Therefore V_{PP} is designated at 25V ±1V. When V_{PP} exceeds the maximum rating (including overshoot), the p-n junction of the device sometimes leads to permanent breakage of the element. Taking this point into consideration, please take sufficient care by performing checking of V_{PP} over shoot of the P-ROM writer, etc.
Since a total inspection cannot be performed prior to shipment on matters such as writing & erasing cycles, a guarantee form is not employed but it maintains a standard capable of repeating more than 100 times normally. It can be said to be a sufficient standard when considering the repetition to be about 10 times in maximum in actual use.

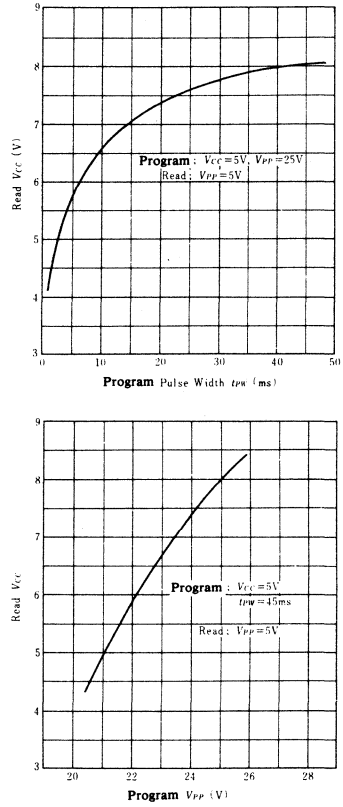


Fig. 2 HN462716 Typical Programming Characteristics

1.2 Erasing

Data erasing of HN462716 is performed by the discharge of the electric charge in the floating gate and with the ultraviolet ray irradiation to the memory cell.
The erasing condition of HN462716 is stipulated as ultraviolet ray wavelength 2,537Å and minimum integrated dose 15W.sec/cm^2. This condition can be obtained by placing an ultra violet lamp of 12,000μW/cm^2 within 1 inch of the device and shelving it for about 20 minutes. The material quality of the transparent lid is sapphire and the transmission factor of the ultravioletrays is about 70%. However, when contamination and foreign matters exist on the cap surface, the transmission factor will deteriorate and the time required for erasing will become extended. In such a case, it is necessary to remove the contamination with solvents such as alcohol, etc., which do not affect the package. Actually, erasing of the element can be sufficiently performed in a shorter time than the stipulated erasing time but since the erasing condition of 15W.sec/cm^2 for performing erasing with a sufficient margin within the device usage condition range has been decided, always be sure to perform irradiation above this condition.

Although the efficiency of ultraviolet rays of a wavelength of less than 3,000 ~ 4,000Å may differ, it has the capability of discharging the electric charge accumulated in the memory cell of HN462716. The typical erasing characteristics of HN462716 are shown in Fig. 3. The existance of easy-to-erase and hard-to-erase bits in the LSI in this drawing is due to the disperison of accumulated electron volume, etc.

Since a slight a mount of ultraviolet rays is contained in fluorescent lights and sunlight, there lies a possibility of causing inversion ("0" → "1") of the memory information accompanying the vanishing of the charge when such light is irradiated for a long period. Therefore, when there lies a possibility of light being irradiated and a high reliability is demanded, provide measures for shielding the light such as pasting a seal on the lid, etc.

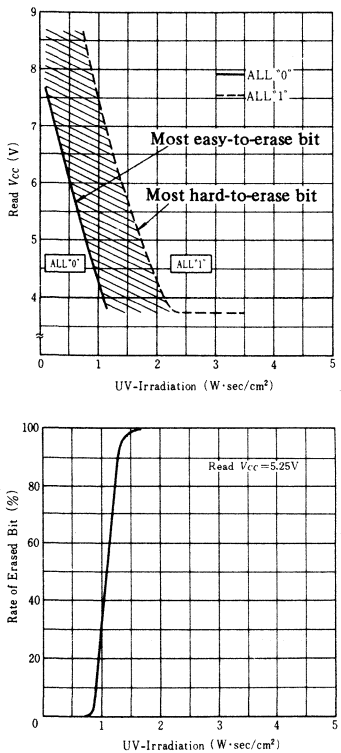


Fig. 3 HN462716 Typical Erasing Characteristics

1.3 EPROM Writer

The 16K EPROM writer stores the program in its internal RAM and writes the program in the EPROM. For this programming, the minimum of 3 functions, the Blank check function prior to programming, the programming function and the Verify function after programming are necessary.

The programming flow is as shown in the following drawing. As shown in the drawing, there are also writers provided with a reverse insertion checking function or pin contact checking function prior to the Blank Check.

The outline of each block is as follows.

(a) Pin contact check

In the connection test of the ROM pin and the socket, normally checking is performed by detecting the forward current of each EPROM pin.

Care is necessary as this forward biased resistance differs according to products of each company.

(b) Reverse insertion check

This check detects the reverse insertion of the device, places the equipment in reset mode and protects the device and equipment.

(c) Blank check

This check is performed prior to programming and checks whether or not it is an erased EPROM or for preventing EPROM reprogramming.

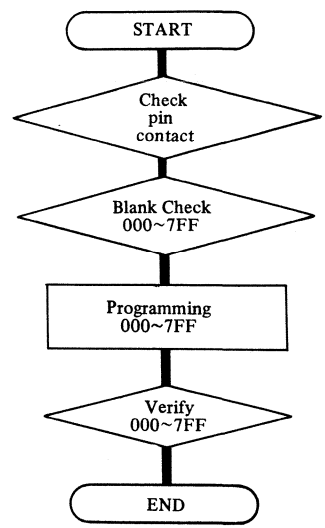
Since the output data in the erased condition are "1" (high level) in case of HN462716, check whether or not data in EPROM are all "1". It will fail-stop even when 1 bit is of "0" (low level).

Normally, it is designed to provide warning with a lamp or buzzer.

(d) Programming

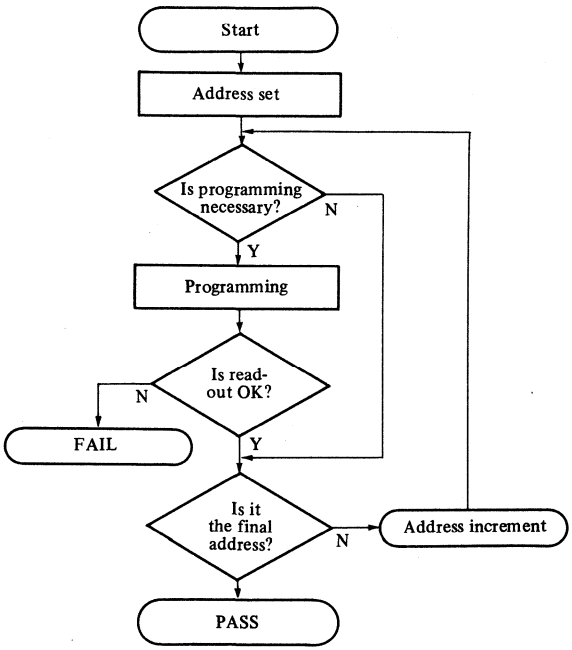
The function of programming the data in the internal RAM of the writer into EPROM and will fail-stop when programming cannot be made.

The normal flow is as shown below. The EPROM data will be read out prior to programming and compared with the programming data. If they coincide, programming will be skipped and if they differ, programming will be performed. Then, read out will be made again and compared with the programming data, and if they coincide, it will progress to the next address.



(e) Verify

This function is for checking after programming completion whether or not the programming is correct when comparing with the data in the internal RAM of the writer and it performes fail-stop when it does not coincide. Normally, when it fails, together with lighting of the fail lamp, the address and data are displayed.



(f) How to input the program

There are the following methods for inputing the program data to the internal RAM of the writer.

Normally, paper tape input and teletypewriter input are options.

Method	Content
Copy input	Input by copying the master ROM.
Manual input	Input by the keyswitch of the front panel. Used for correction or revision of program
Paper tape input	Read the paper tape furnished from the host system with the tape reader
Teletypewriter input	Input with the teletypewriter. Preparation, correction and list preparation of the program can be made.

1.4 Handling of EPROM

1.4.1 Malfunction caused by static charge

There is a possibility of static charge generating on the glass window of EPROM leading to malfunction of the LSI when the glass surface of EPROM is touched by charged human body or rubbed with plastic or dried cloth. Typical malfunctions are blank fail, write margin fail, etc., which look as if writing has been made in the LSI. This subject has already been mentioned at the international society on LSI reliability and the cause lies in the fact that a charge generates on the chip of LSI due to static charge on the window and this charge remains for a prolonged period.

1.4.2 Regeneration method of charged LSI

When EPROM is accidentally charged and the above-mentioned fail has occurred, the LSI can be completely regenerated to blank condition by irradiating with ultraviolet rays for erasing for a prescribed time. The charge remaining on the chip differs from that accumulated on the floating gate and normally, practically all charges are neutralized when ultraviolet rays of about 50 mW.s/cm^2 are irradiated. Therefore, when static charge fail occurs on EPROM in which the program has been written, it is possible to remove the residual charge on the chip surface without changing the programmed pattern by irradiating ultraviolet rays slightly (about 5 ~ 10 seconds in case of 6.5 mW/cm^2). However, since a slight amount of the charge stored in the floating gate will also be discharged in this case, it is necessary to take care not to apply an "overdose" of ultraviolet rays.

1.4.3 Caution in handling

Since the basic cause is the static charge on the window, its prevention is the most important measure in handling. This is the same as the normal IC electrostatic breakdown measures and the following methods exist.

(1) Earth the operator's body during operation. Do not use gloves, etc., which tend to generate static charge.
(2) Do not rub the glass window with plastic, etc., which are easily cause static charge.
(3) Take care as a slight amount of ion is sometimes contained in the cooling medium spray.
(4) Ultraviolet ray light shielding labels (particularly those containing conductive substances) are also effective from the standpoint of static electricity charge prevention.

1.5 Light Shielding Lable

1.5.1 Light shielding effect

In case the data retaining characteristics is essential when EPROM is used in an environment where there is the possibility of exposure to ultraviolet rays, it is effective to paste a light shielding label having an ultraviolet ray absorption effect on the glass window. A special label for this purpose is being marketed by the EPROM manufacturer, however, those containing metal are generally effective as they absorb ultraviolet rays.

1.5.2 Charge prevention effect

Generally, the possibility of electrostatic charge will be reduced when the surface resistivity is lowered. Since the surface resistance of the sapphire lid is extremely great normally (more than 1515 Ω/□ at 20% humidity), this can lead to static electricity generation. Therefore, if the resistance can be lowered by pasting a light shielding lable, the possibility of charge will decrease.

.5.3 Selection of light shielding lable

ı selecting a suitable light shielding label, it is necessary to ake care about the following points besides the above-men-ioned items.

1) Adhesive property (Mechanical strength)
   Care is necessary in case of reusing the lable or adherence of dust as the bonding force is weakened.
2) Permissible temperature range
3) Moistureproofness

Ipon considering the above points, it is necessary to make uitable selection according to the usage purpose.

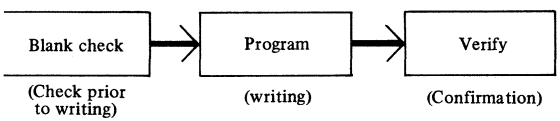
2. Programming of Bipolar PROMs

2.1 Programming Characteristics

The storing system of the Bipolar PROM can be generally lassified into 2 systems; the shortened junction system and use system. Our company employes the shortened junction ystem.

Our products feature the following two points in their pro-ramming characteristics.

- Fast programming speed
  Writing can be made within an average of 1 second in case of 4K bit. When the PROM WRITER is used, the normal operations shown below are successively made; however, only an average 2 ~ 3 seconds are required for each operation in this cycle.



- High programming yield
  Unlike the MOS PROM, the Bipolar PROM cannot be re-generated once, it is written into the memory cell.
  Therefore, it does not allows programming and inspection of the product prior to delivery. Due to this, sometimes a defective product (which does not allow programming) is delivered.
  Generally, the programming efficiency percentage is 90 ~ 95% when programming is performed on the user's side. At our company, special tests such as actually performing programming on the dummy cell in the chip, performing continuity test of all memory cells, etc., are made prior to delivery for minimizing the possibility to deliver defective products.

2.1.1 Access time and power consumpion

Since it uses the oxide isolation technique which has demonstrated excellent results in RAM (Read Write RAM) and employs the SBD (Schottky Barrier Diode) TTL circuit, the following are its features.

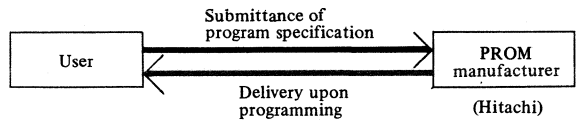
- Fast access time
- Small power consumption
- High reliability

2.2 Programming

There are two methods in the programming method of PROM. That is, the method when programming is made by the PROM manufacturer and delivered and the method when programming is made on the user's side. Both these methods and procedures will be explained below.

2.2.1 Programming performed by the PROM manufacturer

As shown in the drawing below, the manufacturer receives the program specification (specification designating the program pattern) from the user, performs writing (Programming) in accordance with the specification and performs delivery. In this case, a special writing fee is charged.



2.2.2 Programming performed by user

In this case, the following three items must be prepared by the user.

1 PROM WRITER (Main unit of programming equipment)
  One capable of being used in common with equivalent products of other companies.
2 Performance board (Exclusive board designated by each manufacturer)
  Minimum of 1 board for Hitachi PROM.
3 Sockets (sockets suited to product)
  Minimum of one socket per product. These sockets are purchased from the PROM WRITER manufacturer.

The relationship among PROM WRITER manufacturer, Hitachi and user are as shown in Fig. 4.

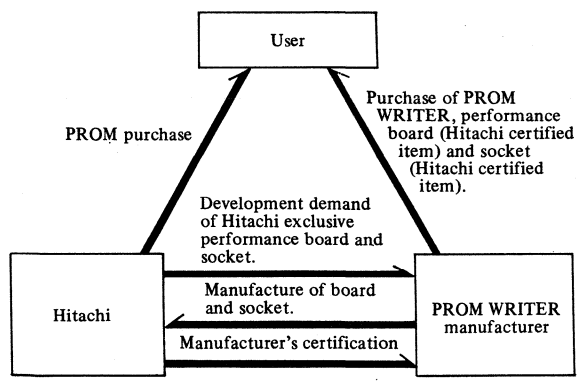


Fig. 4 Relationship among Hitachi, User and PROM WRITER manufacturer

As indicated above, the user purchases the performance board and sockets exclusively for Hitachi products together with purchasing the PROM WRITER.

2.3 Programming Device

There are about ten programming device manufacturers. However, this does not mean that any manufacturer's device will suffice. The reasons are as follows.

- The suitability of the programming device affects the programming efficiency. Therefore, it should be a device of a reliable manufacturer.
- The servicing setup for handling troubles should be consolidated. The setup should be one that judgement can be accurately made on whether it is a writing device trouble or PROM trouble.

Hitachi has prepared a list of recommended manufacturers which meet the above requirements. Please contact us for information in this regard.

■ MASK ROM PROGRAMMING INSTRUCTION

The writing of the custom program code into the mask ROM s performed by the CAD system using a large-sized computer. You should submit the data of the ROM code in conformity with the specification explained below by either paper tape or magnetic tape. In addition, enter your instructions such as the chip select, customer part number, etc., in the "ROM Specification Identification Sheet" and attach it to the ROM code data.

1. Overall Specification

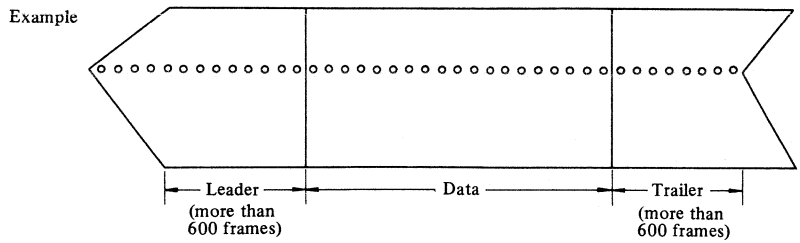
Since the submitted paper tape, card or magnetic tape is fed nto the large-size computer as it is, observe the following specifications.

1.1 Specification of Paper Tape

1.1.1 Any color paper tape may be used as long as it is a marketed 1 inch wide paper tape for computers. However, a black color paper tape is recommended.

1.1.2 Take more than 600 frames for the leader and trailer.

1.1.3 Make the paper tape so that there is one roll for each chip. Since extending the single chip portion over several rolls and entry of several chips in one roll is impermissible, please submit it by compiling into the single-chip portion for each roll.



1.1.4 Parity mode

The presence and type of parity are clearly described in the "ROM Specification Identification Sheet".

There are following modes in the parity system.

(1) With parity
  Even parity . . . . . EVEN
  Odd parity . . . . . ODD
(2) Without parity

1.1.5 Use the 8 unit ASCII code as the code.

1.2 Specification of Magnetic Tape

1.2.1 Use the following type of magnetic tape which can be entered in a magnetic tape device which is compatible with the IBM magnetic tape device.

(1) Length . . . . . 2,400 feet, 1,200 feet or 600 feet
(2) Width . . . . . 1/2 inch
(3) Channel . . . . . 9 channels
(4) Bit density . . 800 BPI or 1,600BPI (Clearly state which it is in the "ROM Specification Indentification Sheet".)

1.2.2 Use the EBCDIC code as the use code.

1.2.3 Make the format of the magnetic tape as described below.

(1) No leading tape mark
(2) No lable
(3) Record size . . . . . 80 byte/1 record
(4) Block size . . . . . 10 records/1 block
(5) The end of the file should be indicated by 2 successive tape marks (TM).

1.2.4 Ensure that the magnetic tape becomes of 1 roll for each chip. Since extending the single-chip portion over several rolls is impermissible, submit by compiling into the single-chip portion for each roll.

2. Data Mode

2.1 HMCS6800 Load Module Mode

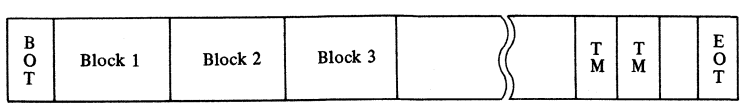
This mode is the object mode output from the assembler of HMCS6800.

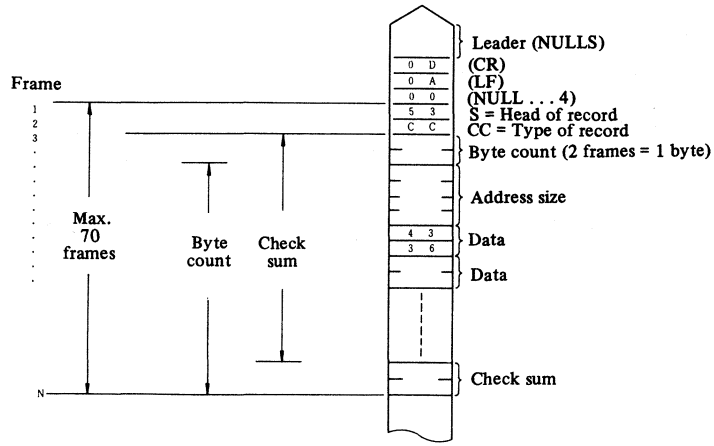
2.1.1 Divide the 8 bit code into the upper and lower 4 bit codes and convert each into hexadecimal notation.

(Example) The code of 1100 0110 becomes as follows under binary notation.

(Upper 4 bits) $D_7D_6D_5D_4$	(Lower 4 bits) $D_3D_2D_1D_0$	Bit weight (ROM output equivalence)
1 1 0 0	0 1 1 0	
C	6	

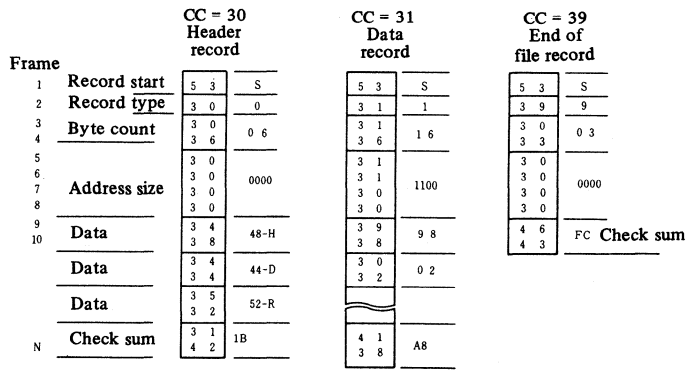
2.1.2 The composition of the load module mode is shown below by taking the case of paper tape as the example. The numbers written in the tape are ASCII code hexadecimal numbers of the data.





(Note) The check sum is a technique which disregards the complement on one of each bit sum of the 8 bits.

2.1.3 The actual load module mode becomes as shown below.



S0 indicates the head of the file and S9 indicates the end of the file. The actual data enters following S1. It means that the data starts from the address (hexadecimal) indicated in the address size. The address of the address size of the data recorder is compared with the next data recorder address by counting in increments of 1 byte of the data and checking whether it is sequential or not. In places where the address is skipped, the data of 00 automatically enters hexadecimally. The printed example of the paper tape of the HMCS6800 load module mode is as shown below.

Example

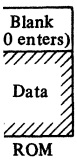
Header record	→S00B000058204558414D504CB5
Data record	→S113F0007EF5587EF7897EFAA77EF9C07EF9C47E24
Data record	→S112F010FA657EFA8B7EFAA07EF9DC7EFA247E06
End of file record	→S9030000FC

2.1.4 The ROM code data are capable of handling the following 4 types of cases. A header recorder is required in front of the data recorder and an end of file recorder at the back of the data recorder.

(1) Case when the data reaches full capacity of ROM

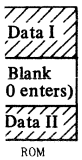
The ROM recorder for 1 chip enters into the data recorder. Since the address of the address size of the data recorder counts the data and checks whether or not it is in a sequential address, it becomes necessary that the address not be skipped. The ROM head address column of the "ROM Specification Identification Sheet" becomes 0.

) Case when data is input from en route of ROM



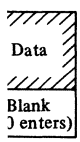
In this case, perform entry by decimal notation in the ROM head address column of the "ROM Specification Identification Sheet" on which ROM address you wish to input the data. The data 00 will automatically enter into the blank address.

) Case when data is input by skipping intermediate address



The address of the address size of the data recorder is counted in increments of 1 byte of the data, compared with the next address of the data recorder and checked whether or not it is sequential. The data 00 automatically enters by hexadecimal notation into the ROM code of the skipped address. Therefore, the writing of data as in the following drawing is also possible. In this case, perform entry into the "ROM Specification Identification Sheet" that the ROM head address enters from 0 address for data I and from which address it enters for data II.

) Case when the data is less than the full capacity of ROM



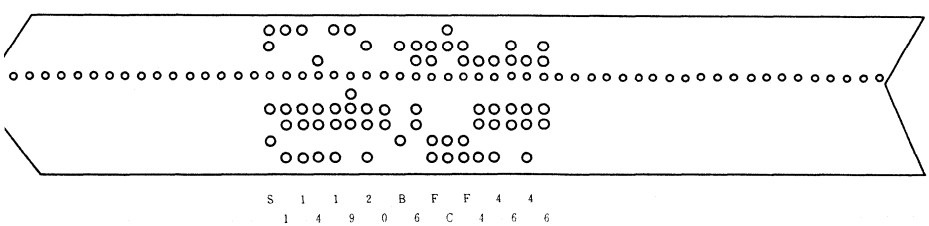
In case the data volume is less than the total byte capacity of ROM LSI when the end of file recorder appears, it becomes written as the ROM code as shown in the following drawing.

Note 1) Sometimes X is used besides P and N in the display of the word content by the BNPF slice.
X means that the user is not concerned whether the bit is P or N. However, since it is necessary to decide the P or N for performing tests, Hitachi performs selection of P or N. The results are informed by making entry in the identification table.

Note 2) The contents of the BNPF slice are not only those with the continuation of PN and the form of B*nF can also be used. This means that the content of the slice existing just prior to this word will be repeated for n words from this word.
For example, when B*4F exists at the 10th word, it means that the content of the 9th word will be repeated in the 10th, 11th, 12th and 13th words. (However, it does not necessarily follow that the X content of Note 1 above will be repeated.) n shall start from 1 and be a number below the total addresses of ROM.

Note 3) When a certain block is not used (when an unused ROM address exists), disposition can be made by utilizing Notes 1 and 2.

xample) Indicates the example of the paper tape when the data recorder is S1141920B6FC ...



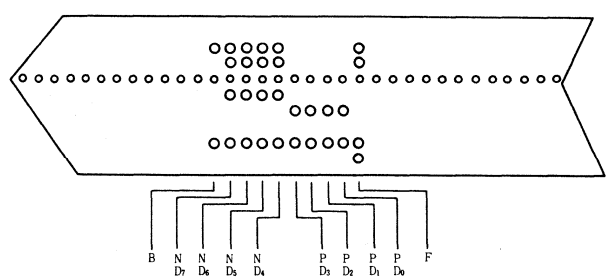
? BNPF Mode

?.1 One word is symbolized by the word start mark B, ? bit content represented by 8 characters of P and N, and ? BNPF slice composed of successive 10 characters of the ?rk end mark F.

?.2 The contents from F of one BNPF slice up to B of the ?xt BNPF slice are ignored.

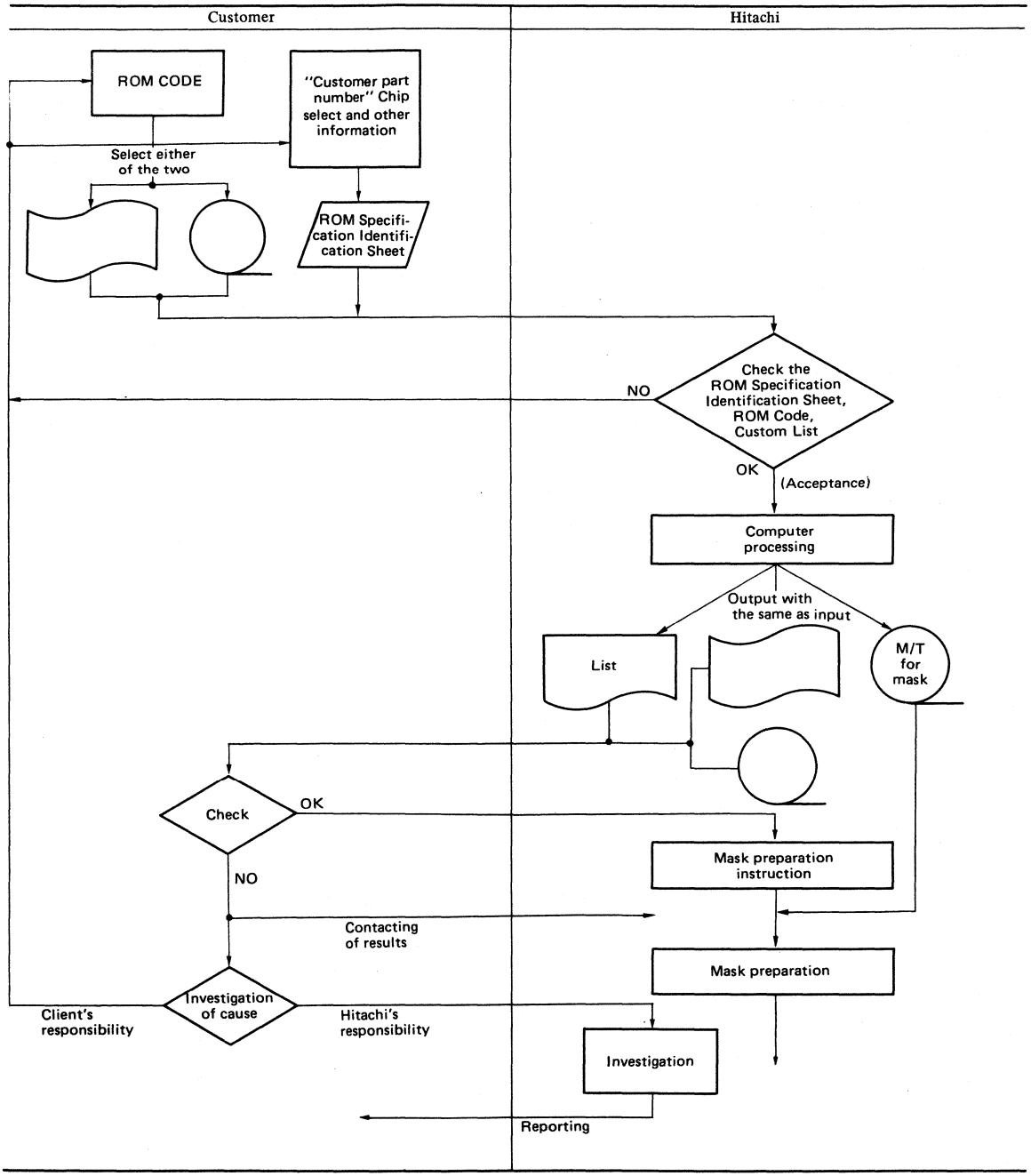
?xample) The code of 0F by hexadecimal notation is symbolized as shown below (in case of paper tape)

?.3 It is necessary to designate the bit pattern (BNPF ?e) on all ROM addresses. Therefore, the term of the ROM ad address of "ROM Specification Identification Sheet" ?ays becomes 0.



. . . . . Indicates start of 1 word.
. . . . . Indicates "0" of 1 bit data.
. . . . . Indicates "1" of 1 bit data.
. . . . . Indicates end or 1 word.

Mask ROM Development Flowchart



I SYMBOLS AND TERMS FOR IC MEMORIES

Terminal Names

Terms	Bipolar		MOS			Memory Support Circuits
	HM2100 Series	HM2500 Series	ROM	Static RAM	Dynamic RAM	
Supply Voltage Terminal	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
					V_{DD}	V_{DD}
					V_{BB}	
				V_{SS}	V_{SS}	
	V_{EE}					
Address Input (Input) Terminal	A_0~A_9	A_0~A_9	A_0~A_{11}	A_0~A_{10}	A_0~A_6	A, B
Data Input Terminal	Din	Din	Din	Din	Din	
Input/Output Terminal				I/O		
Chip Enable Input Terminal				CE		
Chip Select Input Terminal	CS	CS	CS	CS		
Write Enable Input Terminal	WE	WE		WE	WE	
Row Address Strobe Terminal					RAS	
Column Address Strobe Terminal					CAS	
Program Input Terminal			Program			
Data Output (Output) Terminal	Dout	Dout	Dout	Dout	Dout	Y, X
Ground Terminal	GND	GND		GND		GND
Nonconnection			NC		NC	NC

Absolute Maximum Ratings

Terms	Bipolar		MOS			Memory Support Circuits
	HM2100 Series	HM2500 Series	ROM	Static RAM	Dynamic RAM	
Supply Voltage	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
					V_{DD}	V_{DD}
	V_{EE}					
			V_{SS}		V_{SS}	
Terminal Voltage				V_T		
Input Voltage	V_{in}	V_{in}	V_{in}	V_{in}	V_{in}	V_{in}
Output Voltage	V_{out}	V_{out}	V_{out}		V_{out}	
Input Current	I_{in}	I_{in}				
Output Current	I_{out}	I_{out}				
Load Capacitance						C_L
Power Dissipation			P_T	P_T		P_T
Operating Temperature	T_{opr}	T_{opr}	T_{opr}	T_{opr}	T_{opr}	T_{opr}
Storage Temperature	T_{stg}	T_{stg}	T_{stg}	T_{stg}	T_{stg}	T_{stg}

3. DC Characteristics

Terms	Bipolar		MOS			Memory Support Circuits
	HM2100 Series	HM2500 Series	ROM	Static RAM	Dynamic RAM	
Input Logic 1 Voltage	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IH}
Input Logic 0 Voltage	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
Input Logic 1 Threshold Voltage	V_{IHC}				V_{IHC}	
Input Logic 0 Threshold Voltage	V_{ILC}				V_{ILC}	
Output Logic 1 Voltage	V_{OH}	V_{OH}	V_{OH}	V_{OH}	V_{OH}	V_{OH}
Output Logic 0 Voltage	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
Output Logic 1 Threshold Voltage	V_{OHC}					
Output Logic 0 Threshold Voltage	V_{OLC}					
Input Logic 1 Current	I_{IH}	I_{IH}	I_{IH}			I_{IH}
Input Logic 0 Current	I_{IL}	I_{IL}				I_{IL}
Input Current		I_I				I_I
Input Leakage Current			I_{LI}	I_{LI}	I_{LI}	
Input Logic 0 Threshold Current	I_{ILC}					
Output Logic 1 Current		I_{OH}				
Output Leakage Current			I_{LO}	I_{LO}	I_{LO}	
		I_{CEX}				
Output Leakage Current (at High Impedance)		I_{LOK}				
Output Short-circuit Current		I_{OS}				
Input Clamp Voltage		V_I				

4. AC Characteristics
4.1 Recommended Operating Condition

Terms	Bipolar		MOS			Memory Support Circuits
	HM2100 Series	HM2500 Series	ROM	Static RAM	Dynamic RAM	
Time Between Refresh					t_{REF}	
Address Setup Time					t_{AS}	
Address Hold Time					t_{AH}	
CE Off-to-Output High Impedance State					t_{CF}	
Chip Enable Off Time					t_{SB}	
Chip Enable Transition Time					t_T	

2 Read Mode/Cycle

Terms	Bipolar		MOS			Memory Support Circuits
	HM2100 Series	HM2500 Series	ROM	Static RAM	Dynamic RAM	
Read Cycle Time			t_{RC}	t_{RC}	t_{RC}	
Address Access Time	t_{AA}	t_{AA}	t_{ACC}	t_{A}	t_{ACC}	
Chip Select Access Time	t_{ACS}	t_{ACS}		t_{ACS}		
Chip Select Recovery Time	t_{RCS}	t_{RCS}				
Chip Select Delay Time			t_{CS}			
Output Deselect Time			t_{OD}			
Chip Enable On Time			t_{CE}		t_{CE}	
Previous Read Data Valid			t_{OH}	t_{OH}		
Chip Enable to Output Time			t_{CO}	t_{CO}		
WE Setup Time					t_{WL}	
WE Hold Time					t_{WC}	

.3 Write Mode/Write Cycle/Read Modify Write Cycle

Terms	Bipolar		MOS			Memory Support Circuits
	HM2100 Series	HM2500 Series	ROM*	Static RAM	Dynamic RAM	
Write Cycle Time				t_{WC}	t_{WC}	
Read/Write Cycle Time					t_{RWC}	
Read Modify Write Cycle Time					t_{WP}	
Write (Read/Write) Pulse Width	t_{W}	t_{W}	t_{PW}	t_{W}	t_{W}	
Data Setup Time	t_{WSD}	t_{WSD}	t_{DS}	t_{DW}	t_{DW}	
Data Hold Time	t_{WHD}	t_{WHD}	t_{DH}	t_{DH}	t_{DH}	
Address Setup Time	t_{WSA}	t_{WSA}	t_{AS}	t_{AW}		
Address Hold Time	t_{WHA}	t_{WHA}	t_{AH}			
Chip Select Setup Time	t_{WSCS}	t_{WSCS}	t_{CSS}			
Chip Select Hold Time	t_{WHCS}	t_{WHCS}	t_{CS}			
Write Disable Time	t_{WS}	t_{WS}				
Write (Read/Write) Recovery Time	t_{WR}	t_{WR}		t_{WR}		
Output Disable Delay Time			t_{DF}			
Program-to-Read Delay Time			t_{DPR}			
Write-to-Chip Select Delay Time				t_{WCS}		
Chip Select Pulse Width				t_{CS}		
Write Setup Time				t_{DSW}		
Chip Enable On Time					t_{CE}	
Write Reset Time				t_{CW}	t_{WRS}	
Write Hold Time					t_{WH}	
Write Delay Time					t_{WD}	

* Program Operation

4.4 Switching Characteristics

Terms	Bipolar		MOS			Memory Support Circuits
	HM2100 Series	HM2500 Series	ROM	Static RAM	Dynamic RAM	
Rise Time	t_r					t_{TLH}
Fall Time	t_f					t_{THL}
Delay Time (Rising)						t_{DLH}
Delay Time (Falling)						t_{DHL}

4.5 Capacitances

Terms	Bipolar		MOS			Memory Support Circuits
	HM2100 Series	HM2500 Series	ROM	Static RAM	Dynamic RAM	
Input Capacitance	C_{in}	C_{in}	C_{in}	C_{in}	C_{in}	
Output Capacitance	C_{out}	C_{out}	C_{out}	C_{out}	C_{out}	
Address Capacitance			C_{AD}		C_{AD}	
Chip Enable Capacitance			C_{CE}		C_{CE}	
Chip Select Capacitance					C_{CS}	
Write Enable Capacitance					C_{WE}	

■ TERMINOLOGY, SYMBOLS AND DEFINITION BASED ON JEDEC STANDARD FOR SEMICONDUCTOR MEMORY DATA SHEET

The definition of this standard for memory data sheet was established by JEDEC. The use of this is recommended by JEDEC for any new devices.
In this data book, the hitherto used definitions and JEDEC definitions are given of 16K RAM (HM4716A Series).
A summary description of JEDEC Standard is discussed below.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

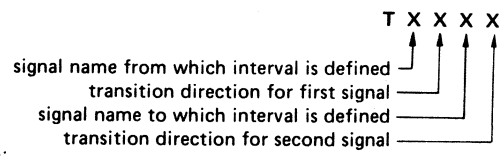
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurement. Examples:

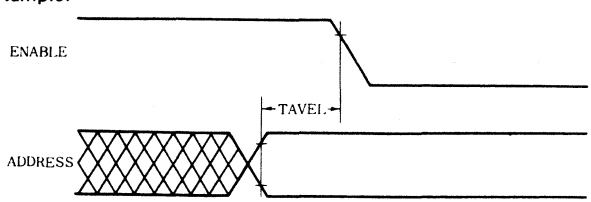
VOH = Output high voltage
IIL = Input low current
IOZ = Output off current (leakage)

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscriptors. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a 'from-to' sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



Example:



The drawing shows the address setup time defined as TAVEL, Address Valid to Enable Low time.

The signal definitions used in this data sheet are:

A = Address
D = Data In
Q = Data Out
W = Write Enable
RE = Row Address Strobe
CE = Column Address Strobe
S = Chip Select

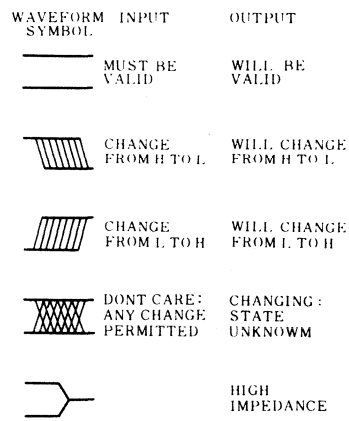
The transition definitions used in this data sheet are:

H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS



DATA SHEETS

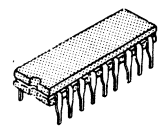
MOS STATIC RAM

HM472114A-1, HM472114A-2, HM472114AP-1, HM472114AP-2

1024-word × 4-bit Static Random Access Memory

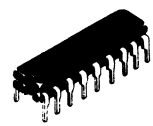
- Fast Access Time . . . . . HM472114A-1 150ns (max.)
  HM472114A-2 200ns (max.)
- Low Operating Power . . . . . 200mW (typ.)
- Single +5V Supply
- Completely Static Memory . . . . . No Clock or Refresh Required
- Fully TTL Compatible . . . . . All Inputs and Output
- Common Data Input and Output Using Three-state Outputs
- N-channel Si Gate MOS Technology
- Pin Equivalent with Intel 2114L Series

HM472114A-1, HM472114A-2



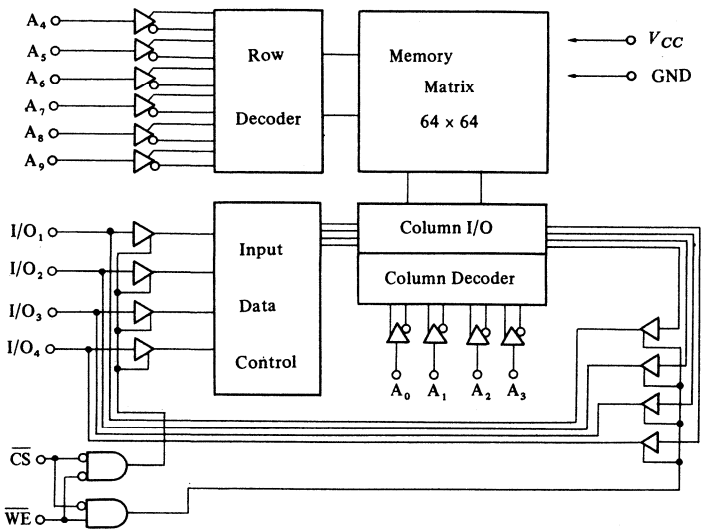
(DG-18)

HM472114AP-1, HM472114AP-2

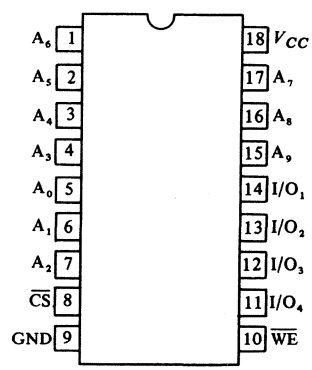


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Terminal Voltage*	V_T	−0.5 to +7	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C

* In respect to GND.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.5	—	0.8	V
	V_{IH}	2.0	—	V_{CC}+1.0	V
Operating Temperature	T_{opr}	0	—	70	°C

■ DC AND OPERATING ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70℃)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}=0~5.5V	—	—	10	μA
I/O Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=2.0V, $V_{I/O}$=0.4V~V_{CC}	—	—	10	μA
Supply Current	I_{CC}	V_{in}=5.5V, $I_{I/O}$=0mA	—	35	60*	mA
Input Voltage	V_{IL}		−0.5	—	0.8	V
	V_{IH}		2.0	—	V_{CC}+1.0	V
Output Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
	V_{OH}	I_{OH}=−0.6mA(V_{CC}=4.5V)	2.4	—	—	V
		I_{OH}=−1.0mA(V_{CC}=4.75V)	2.4	—	—	

Note) *: in respect to HM472114A-2. This value of HM472114A-1 is 70mA.

■ CAPACITANCE (Ta=25℃, f=1MHz)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	3	5	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	5	7	pF

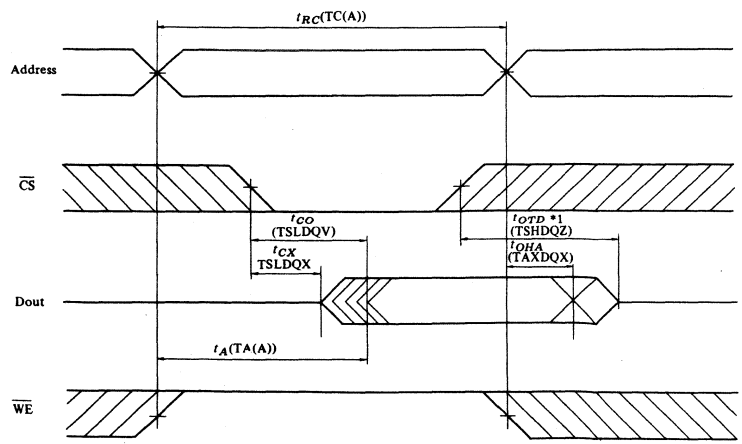
■ AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70℃)

- **AC TEST CONDITIONS**

Input Pulse Levels ..... 0.8V to 2.4V
Input Rise and Fall Times 10ns
Input and Output Timing Levels 1.5V
Output Load ..... 1 TTL Gate and C_L = 100pF

- **READ CYCLE**

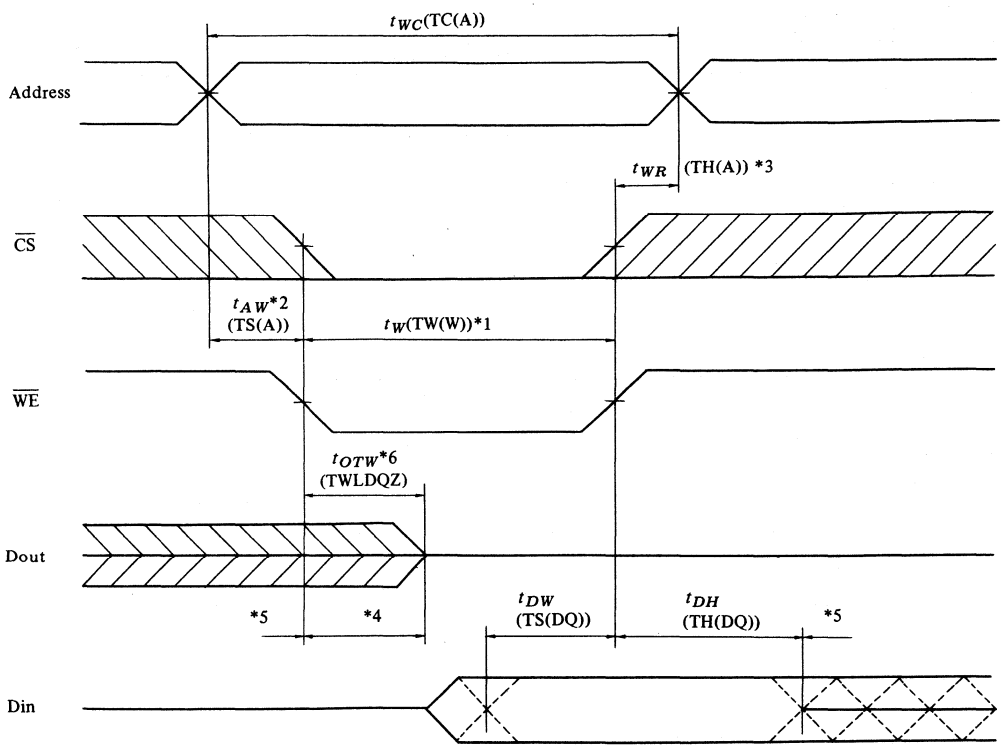
Item	Symbol	HM472114A-1		HM472114A-2		Unit
		min.	max.	min.	max.	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Access Time	t_A	—	150	—	200	ns
$\overline{CS}$ to Output Valid	t_{CO}	—	70	—	70	ns
$\overline{CS}$ to Output Active	t_{CX}	10	—	10	—	ns
Output 3-state from Deselection	t_{OTD}	—	60	—	60	ns
Output Hold from Address Change	t_{OHA}	20	—	50	—	ns



NOTE: 1) t_{OTD} defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

• WRITE CYCLE

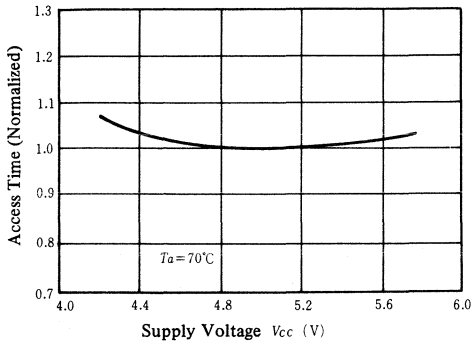
Item	Symbol	HM472114A-1		HM472114A-2		Unit
		min.	max.	min.	max.	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Address to Write Setup Time	t_{AW}	20	—	20	—	ns
Write Pulse Width	t_W	120	—	120	—	ns
Write Release Time	t_{WR}	0	—	0	—	ns
Output 3-state from Write	t_{OTW}	—	60	—	60	ns
Data to Write Time Overlap	t_{DW}	70	—	120	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns



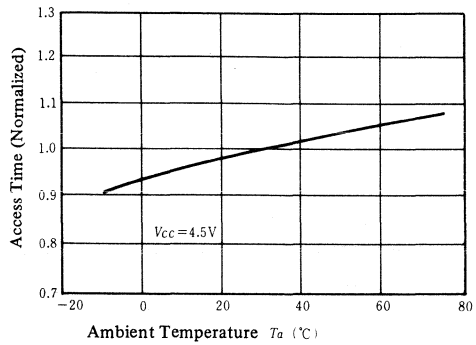
NOTE:

1) A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_W).
2) t_{AW} is measured from the address setting to the latter of $\overline{CS}$ or $\overline{WE}$ going low.
3) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4) During this period I/O pins are in the output state, so that the input signals of opposite phase to the outputs must not be applied to them.
5) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the input signals of opposite phase to the outputs must not be applied to them.
6) t_{OTW} defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

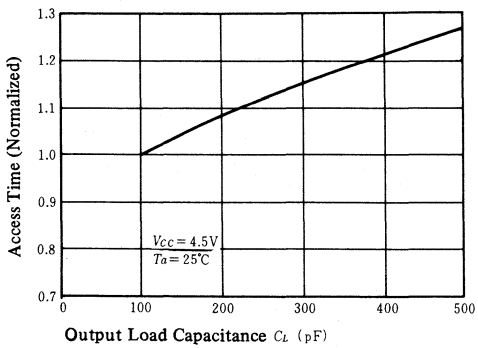
ACCESS TIME vs. SUPPLY VOLTAGE



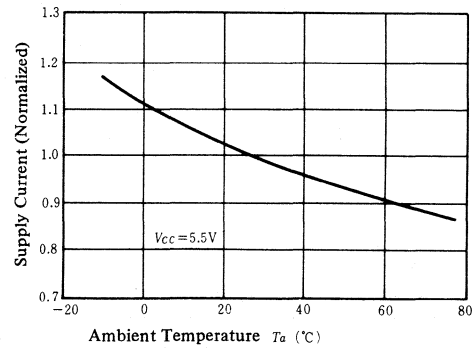
ACCESS TIME vs. AMBIENT TEMPERATURE



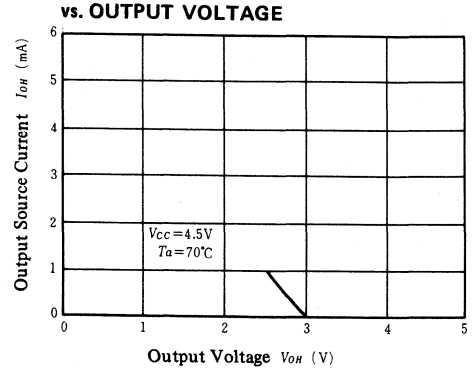
ACCESS TIME vs. OUTPUT LOAD CAPACITANCE



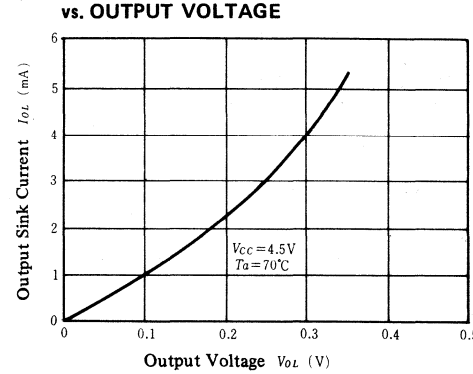
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

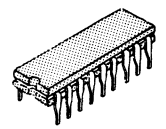


HM472114-3,HM472114-4, HM472114P-3,HM472114P-4

1024-word×4-bit Static Random Access Memory

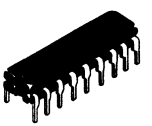
- Fast Access Time ..... HM472114-3 300ns (max.)
  HM472114-4 450ns (max.)
- Low Operating Power ..... 200mW (typ)
- Single +5V Supply Voltage
- Completely Static Memory ..... No Clock or Refresh Required
- Directly TTL Compatible ..... All Inputs and Outputs
- Common Data Inputs and Output
- Three-state Outputs
- DC Standby Mode ..... Reduces V_{CC}
- N-channel Si Gate MOS Technology
- Interchangeable with Intel 2114L Series

HM472114-3, HM472114-4



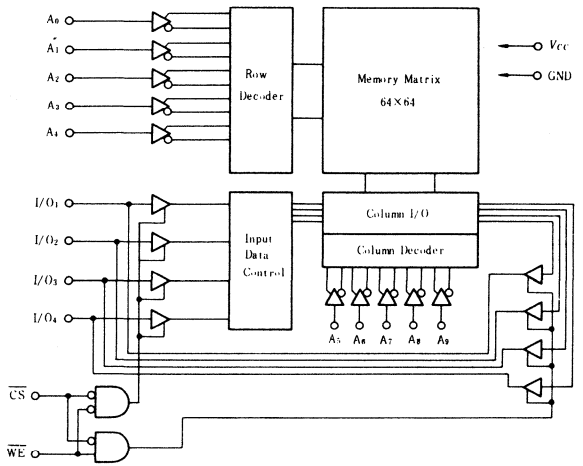
(DG-18)

HM472114P-3, HM472114P-4

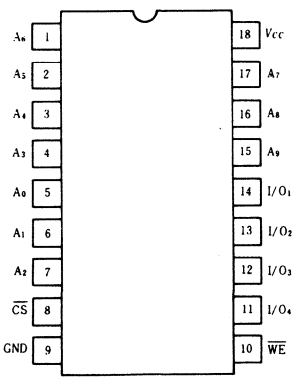


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Terminal Voltage	V_T	−0.3 to +7	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	℃
Storage Temperature (Plastic)	T_{stg}	−55 to +125	℃

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.0	—	V_{CC}+1.0	V
Operating Temperature	T_{opr}	0	—	70	℃

HITACHI

■ DC AND OPERATING ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~+70℃)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}=0~5.5V	—	—	10	μA
I/O Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=2.0V, $V_{I/O}$=0.4~V_{CC}	—	—	10	μA
Supply Current	I_{CC}	V_{in}=5.5V, $I_{I/O}$=0mA	—	35	60	mA
Input Voltage	V_{IL}		-0.5	—	0.8	V
	V_{IH}		2.0	—	V_{CC}+1.0	V
Output Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
	V_{OH}	I_{OH}= -0.6mA, V_{CC}=4.5V	2.4	—	—	V
		I_{OH}= -1.0mA, V_{CC}=4.75V	2.4	—	—	

■ CAPACITANCE (Ta=25℃, f=1MHz)

Item	Symbol	Test Condition	min.	typ.	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	3	5	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	5	10	pF

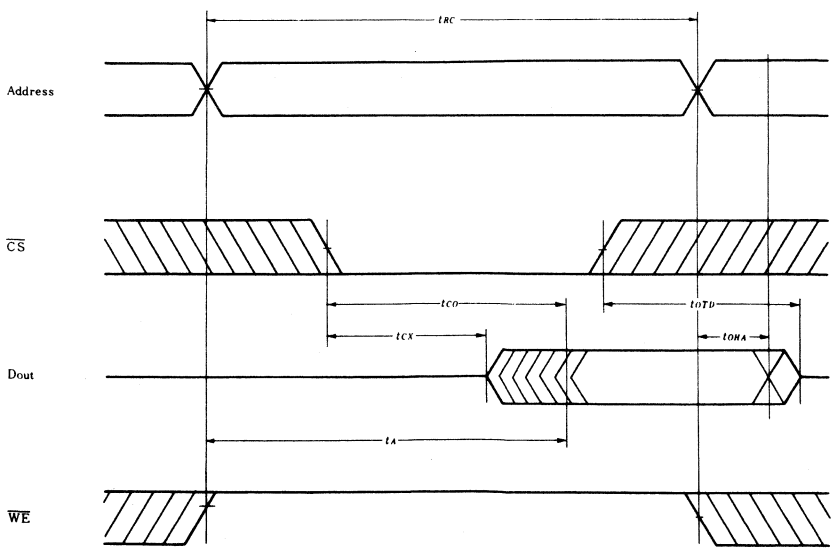
■ AC ELECTRICAL CHARACTERISTICS (Vcc=5V±10%,Ta=0 to +70°C)

• AC TEST CONDITIONS

Input High Levels 2.0V
Input Low Levels 0.8V
Input Rise and Fall Times 10ns
Input and Output Timing Levels 1.5V
Output Load ..... 1 TTL + C_L=100pF

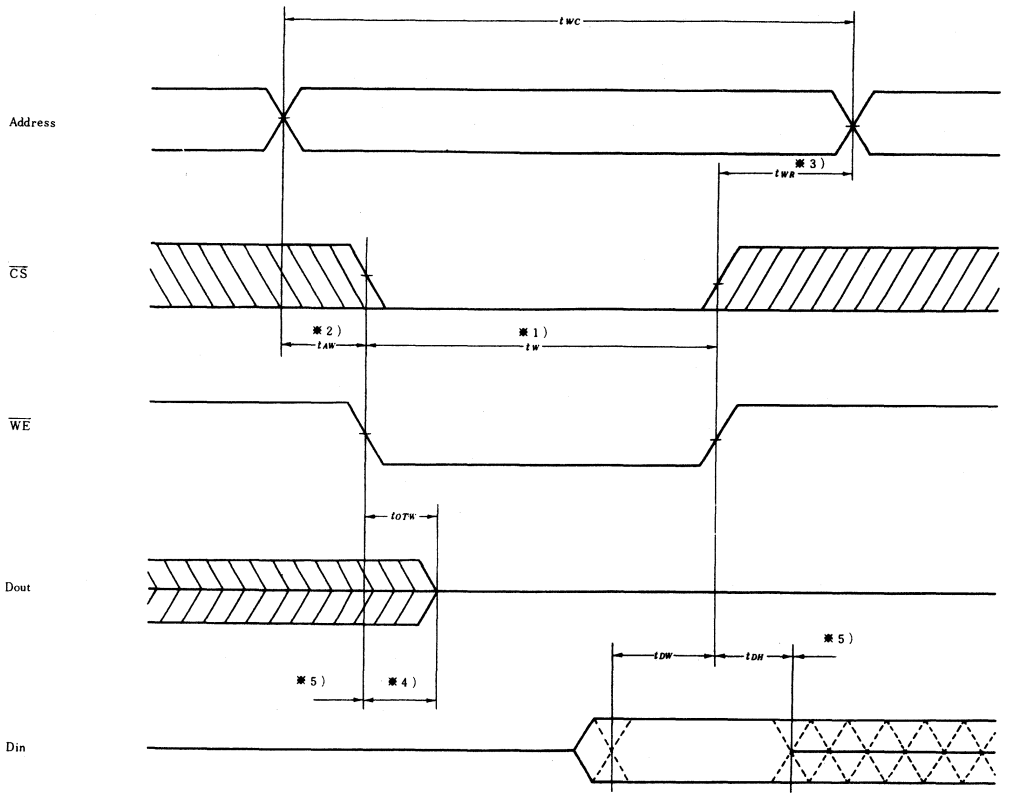
•READ CYCLE

Item	Symbol	HM472114-3, HM472114P-3		HM472114-4, HM472114P-4		Unit
		min.	max.	min.	max.	
Read Cycle Time	t_{RC}	300	—	450	—	ns
Access Time	t_A	—	300	—	450	ns
$\overline{CS}$-to-Output Valid	t_{CO}	—	100	—	120	ns
$\overline{CS}$-to-Output Active	t_{CX}	20	—	20	—	ns
Output 3-state from Deselection	t_{OTD}	-	80	-	100	ns
Output Hold from Address Change	t_{OHA}	50	—	50	—	ns



■ WRITE CYCLE

Item	Symbol	HM472114-3, HM472114P-3		HM472114-4, HM472114P-4		Unit
		min.	max.	min.	max.	
Write Cycle Time	t_{WC}	300	—	450	—	ns
Address to Write Setup Time	t_{AW}	20	—	50	—	ns
Write Pulse Width	t_W	150	—	200	—	ns
Write Release Time	t_{WR}	0	—	0	—	ns
Output 3-state from Write	t_{OTW}	–	80	–	100	ns
Data-to-Write Time Overlap	t_{DW}	150	—	200	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns



Notes: 1) $\overline{CS}$ and $\overline{WE}$ are paced in the WRITE state during low level period (t_W).

2) t_{AW} is an interval from the address setting through fall of the pulse, $\overline{CS}$ or $\overline{WE}$.

3) t_W is from the earlier rise pulse of $\overline{CS}$ or $\overline{WE}$ till the end of the light cycle (t_{WC}).

4) During this period the pulse is output so that the input signal which is the same in phase with the output may be applied to the I/O terminal.

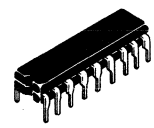
5) During this period, when the $\overline{CS}$ signal is at low level, the pulse is output so that the input signal which is the same in phase with the output data may be applied, if required. Do not however apply the input signal of reverse phase.

HM4334P-3, HM4334P-4

1024-word × 4-bit Static CMOS RAM

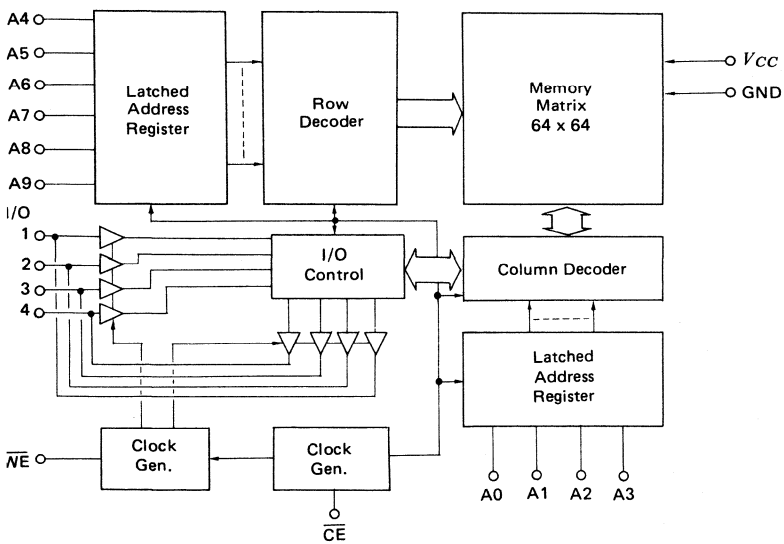
■ FEATURES

- Single 5V Supply
- Low Power Standby and Low Power Operation; Standby: 10 μW (typ.)
  Operation: 20 mW (typ.)
- Fast Access Time; HM4334P-3: 300 ns (max.)
  HM4334P-4: 450 ns (max.)
- Directly TTL Compatible: All inputs and outputs
- Common Data Input and Output using Three-state Outputs
- On Chip Address Register

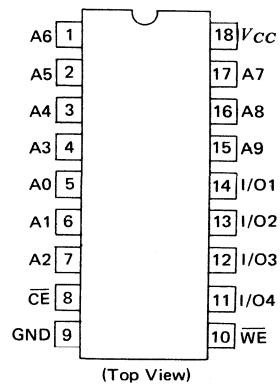


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin *	V_T	−0.3 to Vcc +0.5	V
Power Supply Voltage *	V_{CC}	−0.3 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

* relative to GND

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	HM4334P-3			HM4334P-4			Unit
		min.	typ.	max.	min.	typ.	max.	
Supply Voltage	V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
	GND	0	0	0	0	0	0	V
Input Voltage	V_{IH}	2.4	–	V_{CC} +0.5	2.4	–	V_{CC} +0.5	V
	V_{IL}	−0.3	–	0.8	−0.3	–	0.8	V

■ DC AND OPERATING CHARACTERISTICS

(T_a = 0 to +70°C, GND = 0V, HM4334P-3: V_{CC} = 5V ±5%, HM4334P-4: V_{CC} = 5V ±10%)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	−1.0	–	+1.0	μA
Output Leakage Current	I_{LO}	$\overline{CE}$ = V_{IH}, V_{out} = 0 to V_{CC}	−1.0	–	+1.0	μA
Operating Power Supply Current	$I_{CC}1$	$\overline{CE}$ = 0V, V_{IN} = V_{CC}, $I_{I/O}$ = 0	–	–	1.0	mA
	$I_{CC}2$	$\overline{CE}$ = 0.8V, V_{IN} = 2.4V, $I_{I/O}$ = 0	–	2.5	5.0	mA
Average Operating Current	$I_{CC}3$	V_{IN} ⩾0 or V_{CC}, f = 1MHz, duty 50%, $I_{I/O}$ = 0	–	4	7	mA
Standby Power Supply Current	I_{CCL}	$\overline{CE}$ ≧ V_{CC} −0.2V	–	2	100	μA
Output Voltage	V_{OL}	I_{OL} = 2.0mA	–	–	0.4	V
	V_{OH}	I_{OH} = −1.0mA	2.4	–	–	V

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
I/O Terminal Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	10	pF
Input Capacitance	C_{in}	V_{in} = 0V	–	3	5	pF

■ AC CHARACTERISTICS (T_a = 0 to +70°C, GND = 0V, HM4334P-3: V_{CC} = 5V ±5%, HM4334P-4: V_{CC} = 5V ±10%)

Item	Symbol		HM4334P-3			HM4334P-4			Unit
			min.	typ.	max.	min.	typ.	max.	
Read or Write Cycle Time *	TELEL	t_C	460	–	–	640	–	–	ns
Chip Enable Access Time	TELQV	t_{AC}	–	–	300	–	–	450	ns
Chip Enable to Output Active	TELQX	t_{CX}	50	–	–	50	–	–	ns
Output 3-state from Deselection	TEHQZ	$t_{OFF}1$	–	–	100	–	–	100	ns
Write Enable Output Disable Time	TWLQZ	$t_{OFF}2$	–	–	100	–	–	100	ns
Chip Enable Pulse Width **	TELEH	t_{CE}	300	–	–	450	–	–	ns
Chip Enable Precharge Time	TEHEL	t_P	120	–	–	150	–	–	ns
Address Hold Time	TELAX	t_{AH}	100	–	–	100	–	–	ns
Address Setup Time	TAVEL	t_{AS}	20	–	–	20	–	–	ns
Read Setup Time	TWHEL	t_{RS}	0	–	–	0	–	–	ns
Read Hold Time	TEHWL	t_{RH}	0	–	–	0	–	–	ns
Write Enable Setup Time	TWLEL	t_{WS}	−20	–	–	−20	–	–	ns
$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	TWLEH	t_{WPL}	300	–	–	450	–	–	ns
Chip Enable to Write Enable Delay Time	TELWL	t_{CWD}	300	–	–	450	–	–	ns
Write Enable Hold Time	TEHWH	t_{EWH}	0	–	–	0	–	–	ns
Write Hold Time	TELWH	t_{WH}	300	–	–	450	–	–	ns
Data Input Setup Time	TDVWH TDVEH	t_{DS}	200	–	–	350	–	–	ns
Data Hold Time	TWHDX TEHDX	t_{DH}	0	–	–	0	–	–	ns
Write Data Delay Time	TWLDV	t_{WDS}	100	–	–	100	–	–	ns
Chip Enable Rise/Fall Time	TT	t_T	–	–	300	–	–	300	ns

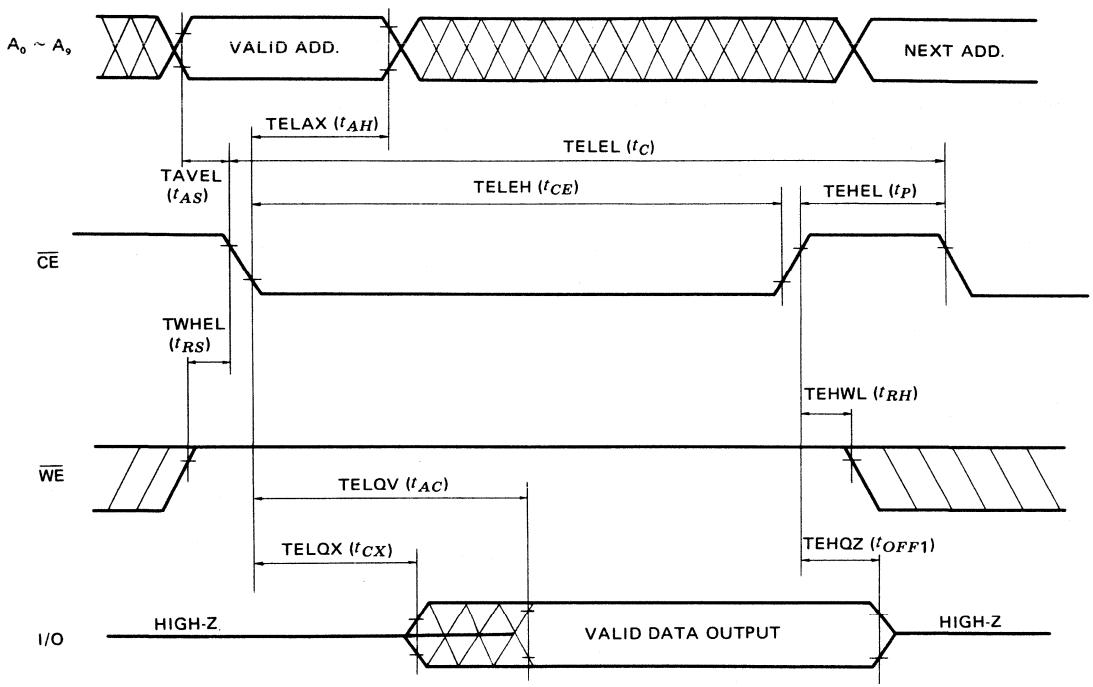
* TELEL (t_C) = TELEH (t_{CE}) + TEHEL (t_P) + t_r (20ns) + t_f (20ns)

** For Read Modify Write Cycle, TELEH (t_{CE}) = TELWL (t_{CWD}) + TWLEH (t_{WPL}) + t_f (20ns)

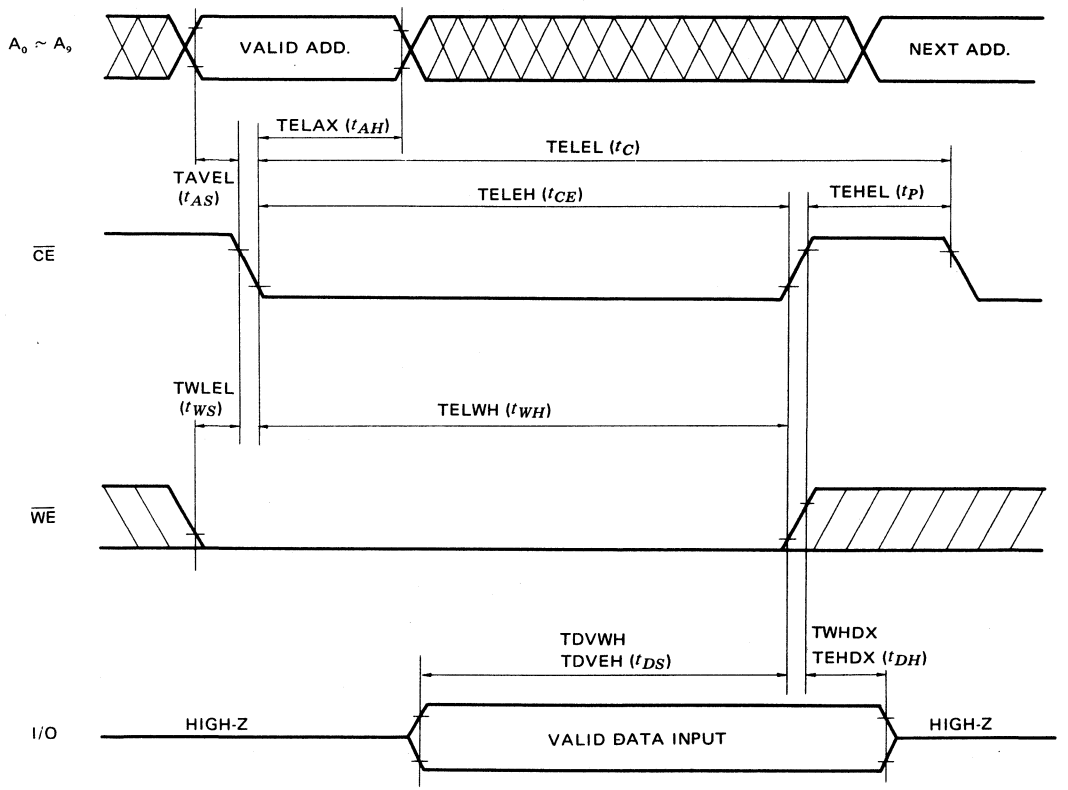
AC TEST CONDITIONS

Input Level	2.4V, 0.8V
Input Rise and Fall Time	20 ns
Timing Measurement Level	2.4V, 0.8V
Reference Level	V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load	1 TTL and C_L = 100 pF

- **READ CYCLE**

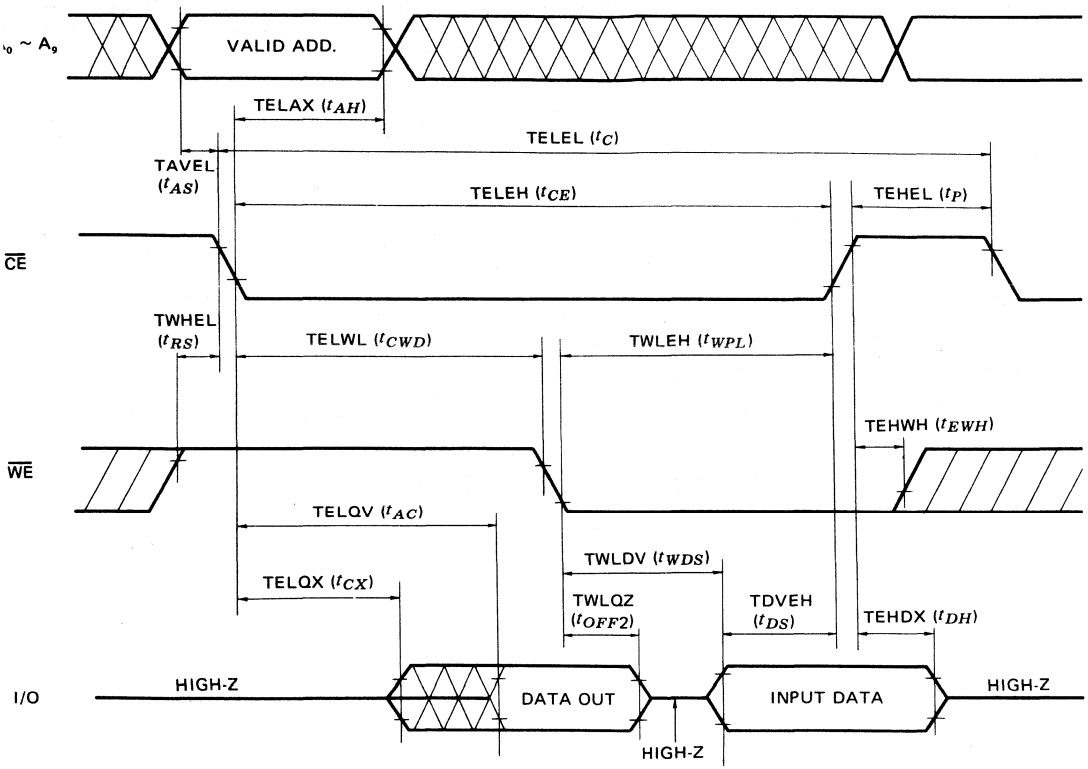


- **WRITE CYCLE**

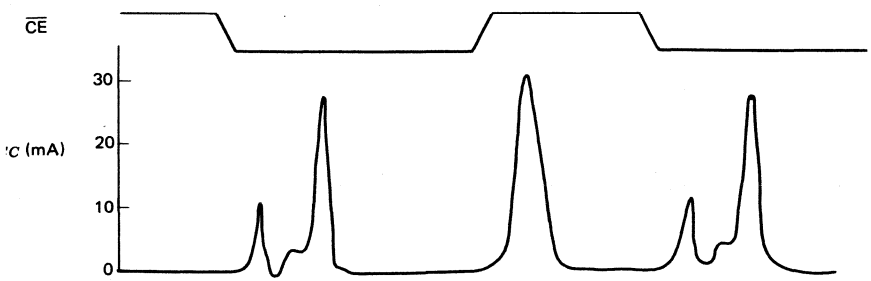


NOTE: t_{DS} and t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

READ MODIFY WRITE CYCLE



CURRENT WAVEFORM



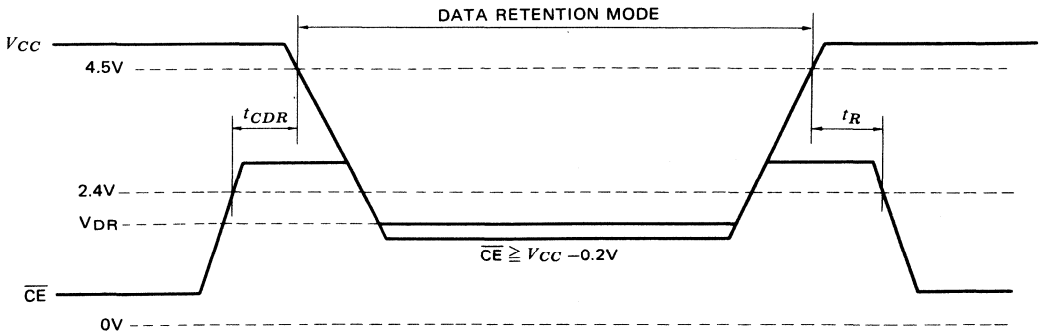
[NOTE] V_{CC} = 5.0V, T_a = 25°C

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

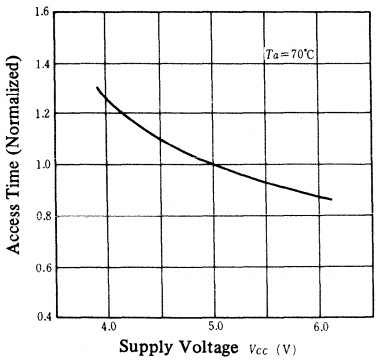
Item	Symbol	Test Condition	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CE} \geqq V_{CC} - 0.2V$	2.0	–	–	V
Data Retention Power Supply Current	I_{CCDR}	V_{DR} = 3.0V	–	0.5	50	μA
Chip Deselection to Data Retention Time	t_{CDR}		0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*	–	–	ns

* t_{RC} = Read Cycle Time

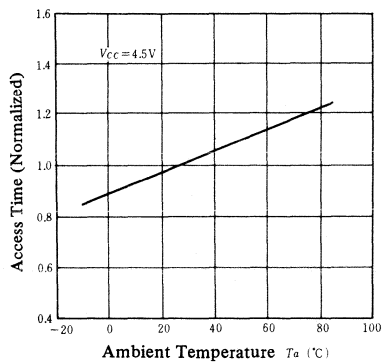
● LOW V_{CC} DATA RETENTION TIMING



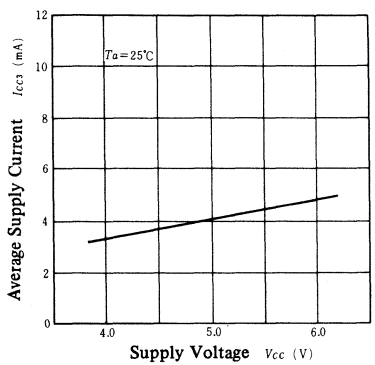
ACCESS TIME vs. SUPPLY VOLTAGE



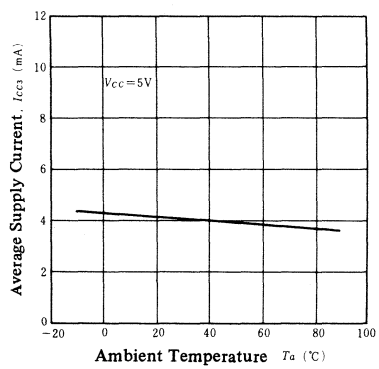
ACCESS TIME vs. AMBIENT TEMPERATURE



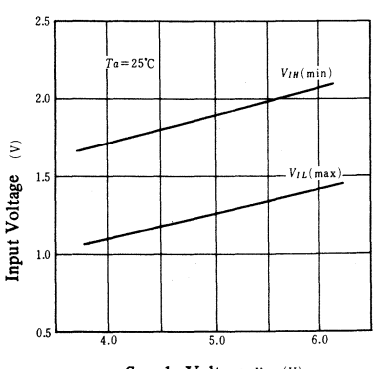
AVERAGE SUPPLY CURRENT vs. SUPPLY VOLTAGE



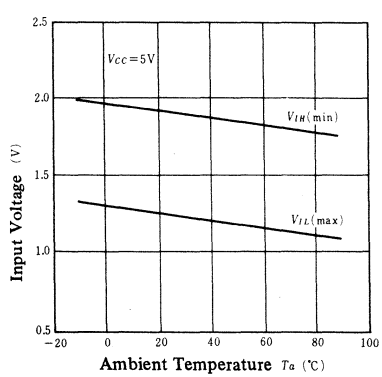
AVERAGE SUPPLY CURRENT vs. AMBIENT TEMPERATURE



INPUT VOLTAGE vs. SUPPLY VOLTAGE



INPUT VOLTAGE vs. AMBIENT TEMPERATURE

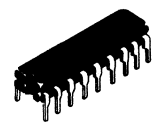


HM6148P, HM6148P-6

1024-word x 4-bit High Speed Static CMOS RAM

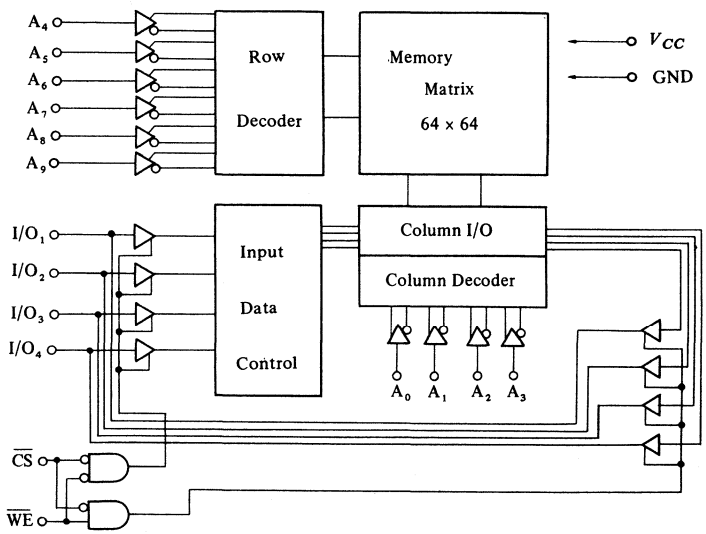
■ FEATURES

- Single 5 V Supply
- Fast Access Time . . . . . HM6148P 70 ns (max)
  HM6148P-6 85 ns (max)
- Low Power Standby and Low Power Operation; Standby : 100 μW (typ)
  Operation : 200 mW (typ)
- Completely Static RAM; No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Three State Output
- Common Data Input and Output
- Pin-Out Compatible with Intel 2148

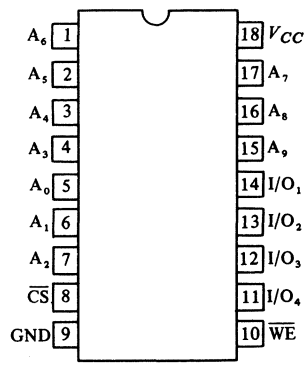


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Terminal Voltage*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature**	$T_{stg(bias)}$	−10 to +85	°C

* In respect to GND.
** Under Bias

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.4	3.5	6.0	V
	V_{IL}	−0.3	–	0.8	V

DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	35	80	mA
Average Operating Current	I_{CC1}	$\overline{CS}$=V_{IL}, Minimum Cycle, Duty=100%, $I_{I/O}$=0mA	–	40	80	mA
	I_{CC2}**	Cycle=150ns, Duty=50%, $I_{I/O}$=0mA	–	35	–	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	5	12	mA
	I_{SB1}	$\overline{CS}$=V_{CC}−0.2V, V_{in}≦0.2V or V_{in}≧V_{CC}−0.2V	–	20	800	μA
Output Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
	V_{OH}	I_{OH}=−3.2mA	2.4	–	–	V

Notes: *: Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
**: Reference only.

CAPACITANCE (T_a=25°C, f=1MHz)

Item	Symbol	Test Condition	min	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	12	pF

(Note) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0 to +70°C, unless otherwise noted)

AC TEST CONDITIONS

Input Pulse Levels . . . . . GND to 3.0V
Input Rise and Fall Times 10ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

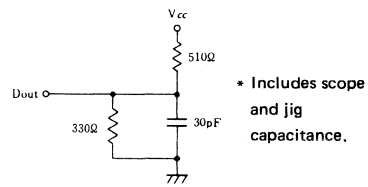


Figure 1. Output Load

READ CYCLE

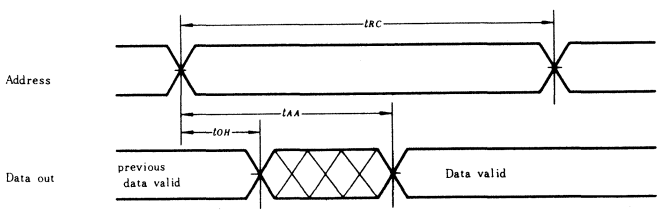
Parameter	Symbol	HM6148P		HM6148P-6		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	70	–	85	–	ns
Address Access Time	t_{AA}	–	70	–	85	ns
Chip Select Access Time	t_{ACS}	–	70	–	85	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}	10	–	10	–	ns
Chip Deselection to Output in High Z	t_{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	40	–	40	ns

■ WRITE CYCLE

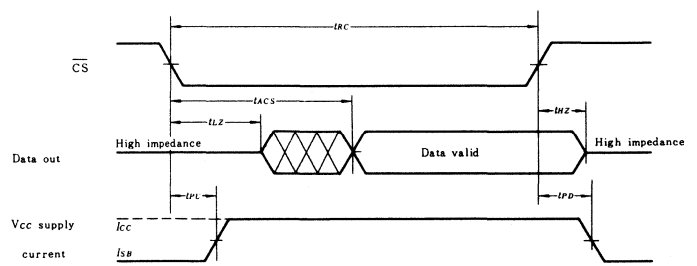
Parameter	Symbol	HM6148P		HM6148P-6		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	70	–	85	–	ns
Chip Selection to End of Write	t_{CW}	50	–	60	–	ns
Address Valid to End of Write	t_{AW}	65	–	80	–	ns
Address Setup Time	t_{AS}	15	–	15	–	ns
Write Pulse Width*	t_{WP1}	50	–	60	–	ns
	t_{WP2}	65	–	80	–	ns
Write Recovery Time	t_{WR}	5	–	5	–	ns
Data Valid to End of Write	t_{DW}	30	–	35	–	ns
Data Hold Time	t_{DH}	5	–	5	–	ns
Write Enabled to Output in High Z	t_{WZ}	0	35	0	45	ns
Output Active from End of Write	t_{OW}	0	–	0	–	ns

Note) *: When the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, I/O pins remain in a high impedance state. In this case t_{WP1}, in the other case t_{WP2} (= $t_{WZ} + t_{DW}$).

● TIMING WAVEFORM OF READ CYCLE NO.1 [1] [2]

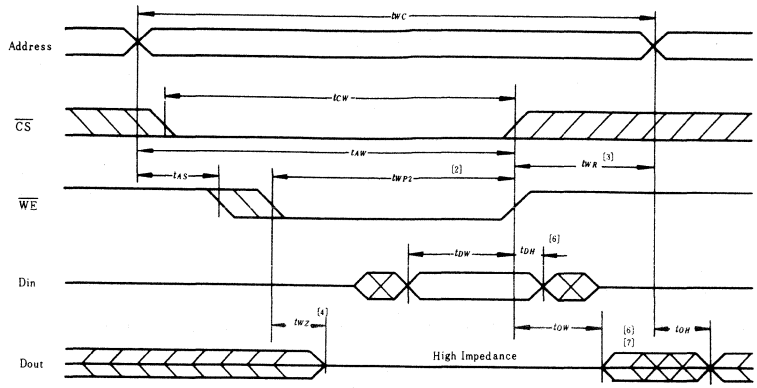


● TIMING WAVEFORM OF READ CYCLE NO.2 [1] [3]

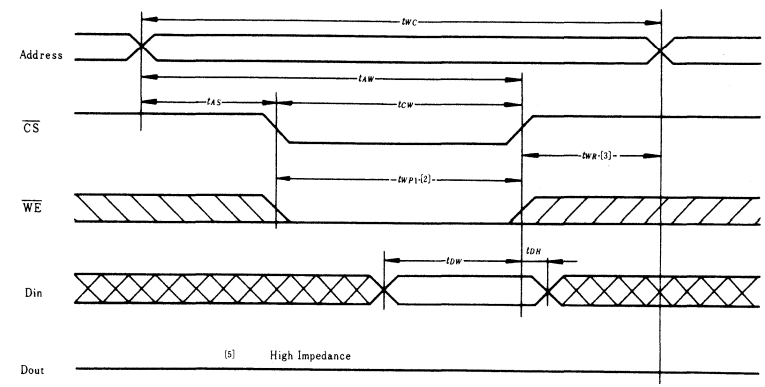


Notes) 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED)[1]



TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED)[1]



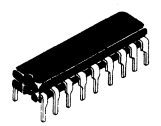
Notes)
1. $\overline{CS}$ and $\overline{WE}$ are paced in the WRITE state during low level period (t_W).
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
6. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
7. Dout is the same phase of write data of this write cycle.

HM6148LP, HM6148LP-6

1024-word x 4-bit High Speed Static CMOS RAM

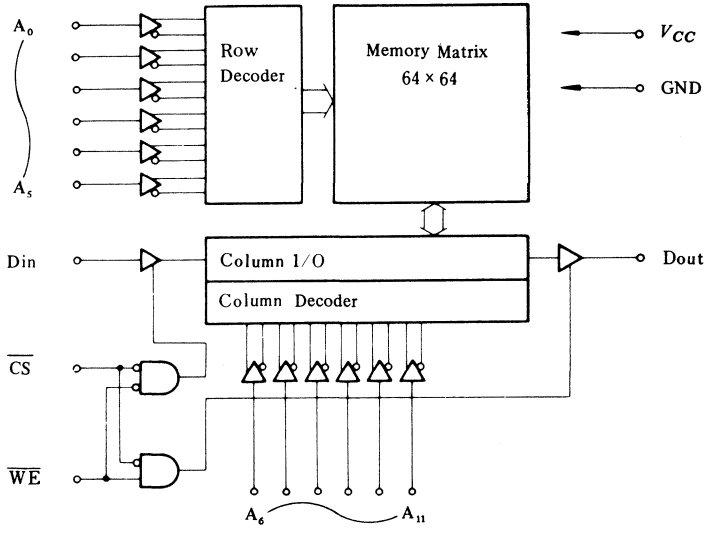
■ FEATURES

- Single 5V Supply
- Fast Access Time ..... HM6148LP 70 ns (max)
  HM6148LP-6 85 ns (max)
- Low Power Standby and Low Power Operation; Standby : 10 μW (typ)
  Operation : 200mW (typ)
- Completely Static RAM; No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Three State Output
- Common Data Input and Output
- Capability of Battery Back Up Operation
- Pin-Out Compatible with Intel 2148

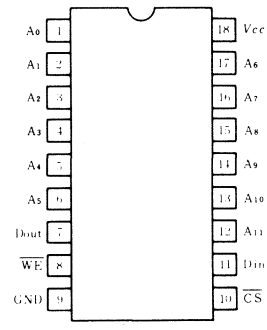


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Terminal Voltage*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature**	$T_{stg(bias)}$	−10 to +85	°C

* In respect to GND.
** Under Bias

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.4	3.5	6.0	V
	V_{IL}	−0.3	–	0.8	V

DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	–	35	80	mA
Average Operating Current	I_{CC1}	$\overline{CS}$ = V_{IL}, Minimum Cycle, Duty = 100%, $I_{I/O}$ = 0mA	–	40	80	mA
	I_{CC2}**	Cycle = 150ns, Duty = 50%, $I_{I/O}$ = 0mA	–	35	–	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	–	5	12	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{in} \leqq 0.2V$ or $V_{in} \geqq V_{CC}-0.2V$	–	1	100	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
	V_{OH}	I_{OH} = −3.2mA	2.4	–	–	V

otes) *: Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
**: Reference only.

CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Test Condition	min	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	12	pF

)te) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

AC TEST CONDITIONS

Input Pulse Levels . . . . . GND to 3.0V
Input Rise and Fall Times . . . . . 10 ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

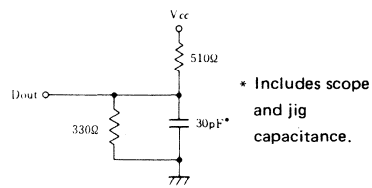


Figure 1. Output Load

READ CYCLE

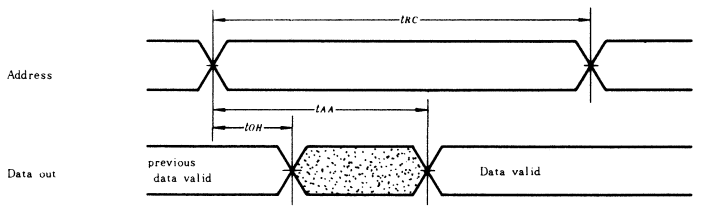
Parameter	Symbol	HM6148LP		HM6148LP-6		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	70	–	85	–	ns
Address Access Time	t_{AA}	–	70	–	85	ns
Chip Select Access Time	t_{ACS}	–	70	–	85	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}	10	–	10	–	ns
Chip Deselection to Output in High Z	t_{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	40	–	40	ns

• WRITE CYCLE

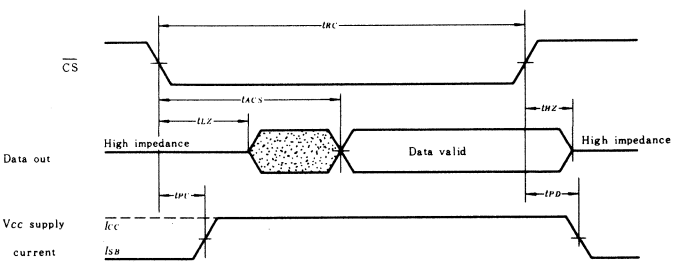
Parameter	Symbol	HM6148LP		HM6148LP-6		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	70	–	85	–	ns
Chip Selection to End of Write	t_{CW}	50	–	60	–	ns
Address Valid to End of Write	t_{AW}	65	–	80	–	ns
Address Setup Time	t_{AS}	15	–	15	–	ns
Write Pulse Width*	t_{WP1}	50	–	60	–	ns
	t_{WP2}	65	–	80	–	ns
Write Recovery Time	t_{WR}	5	–	5	–	ns
Data Valid to End of Write	t_{DW}	30	–	35	–	ns
Data Hold Time	t_{DH}	5	–	5	–	ns
Write Enabled to Output in High Z	t_{WZ}	0	35	0	45	ns
Output Active from End of Write	t_{OW}	0	–	0	–	ns

Note) *: When the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, I/O pins remain in a high impedance state. In this case t_{WP1}, in the other case t_{WP2} (= t_{WZ} + t_{DW}).

• TIMING WAVEFORM OF READ CYCLE NO.1 [1] [2]

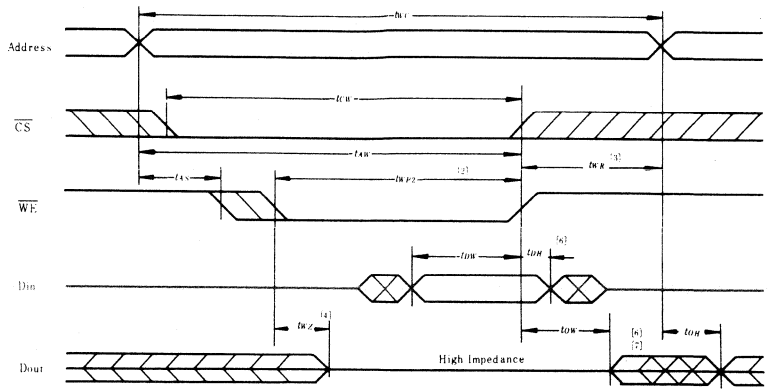


• TIMING WAVEFORM OF READ CYCLE NO.2 [1] [2]

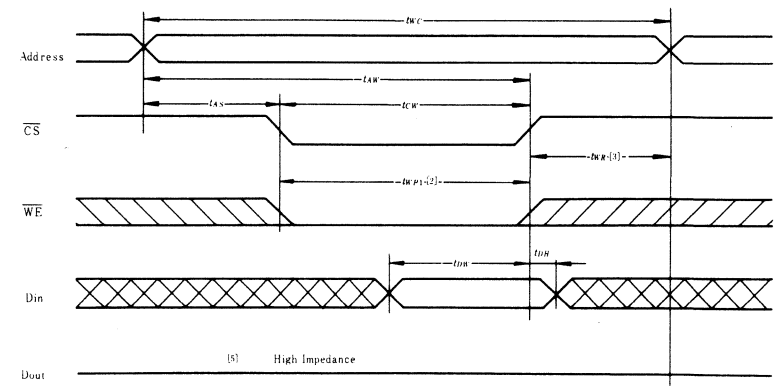


Notes) 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition low.

• TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED) [1]



• TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED) [1]



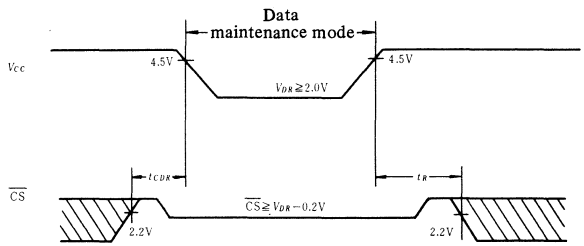
Notes)
1. $\overline{CS}$ and $\overline{WE}$ are paced in the WRITE state during low level period (t_W).
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
6. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
7. Dout is the same phase of write data of this write cycle.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC} - 0.2V$, $V_{in} \geqq V_{CC} - 0.2V$ or $V_{in} \leqq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR}	V_{CC}=2.0V, $\overline{CS} \geqq 1.8V$, V_{in}=1.8V or $V_{in} \leqq 0.2V$	–	–	40	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*	–	–	ns

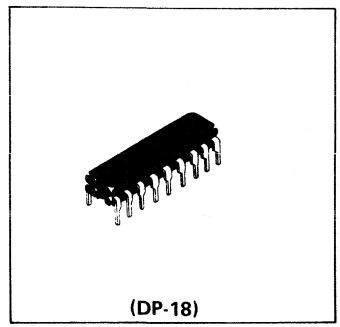
* t_{RC} = Read Cycle Time

• LOW V_{CC} DATA RETENTION WAVEFORM

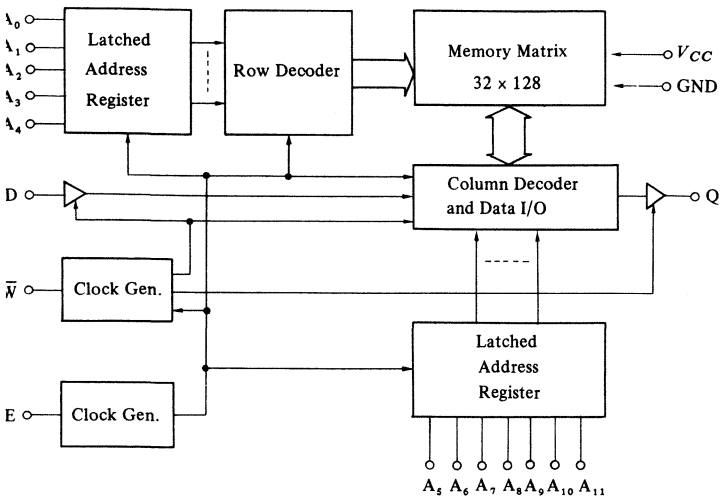


4096-word×1-bit Static Random Access Memory

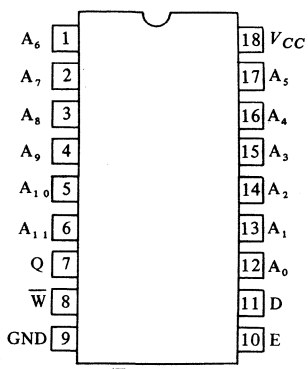
- Low Power Standby . . . . . 10μW typ.
- Low Power Operation . . . . . 20mW typ.
- Data Retention 2.0V
- Fast Access Time . . . . . 450ns max.
- TTL/CMOS Compatible Input/Output
- On Chip Address Register
- Si Gate CMOS Technology



(DP-18)



■ PIN ARRANGEMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Terminal Voltage*	V_T	−0.3 to V_{CC}+0.3	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

with respect to GND

RECOMMENDED DC OPERATING CONDITION (T_a=0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.4	—	V_{CC}+0.3	V
	V_{IL}	−0.3	—	0.8	V

■ DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=0~V_{CC}	−1.0	—	1.0	μA
Output Leakage Current	I_{LO}	E=V_{IL}, V_{out}=0~V_{CC}	−1.0	—	1.0	μA
Operating Power Supply Current	I_{CC1}	E=V_{CC}, V_{IN}=V_{CC} or 0V, Output Open	—	—	1.0	mA
	I_{CC2}	E=2.4V, V_{IN}=2.4V, Output Open	—	2.5	5.0	mA
Average Power Supply Current	I_{CC3}	V_{IH}≧V_{CC} −0.2V, f=1MHz, duty 50%	—	4	10	mA
	I_{CC4}	V_{IH}=2.4V, f=1MHz, duty 50%	—	6	15	mA
Standby Power Supply Current	I_{CCL}	E≦0.2V	—	2	100	μA
Output Voltage	V_{OL}	I_{OL}=2.0mA	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

■ CAPACITANCE (T_a=25°C, f=1MHz)

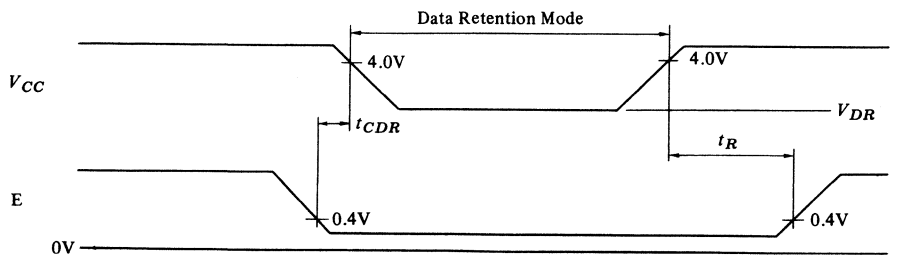
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	3	5	pF
Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	10	pF

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	E≦0.2V	2.0	—	—	V
Data Retention Power Supply Current	I_{CCDR}	E≦0.2V, V_{DR}=2.0V	—	0.5	50	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_C*	—	—	ns

* t_C = Cycle Time

■ LOW V_{CC} DATA RETENTION TIMING



NOTE: All inputs shall be kept below V_{CC}+0.3V under any operating conditions.

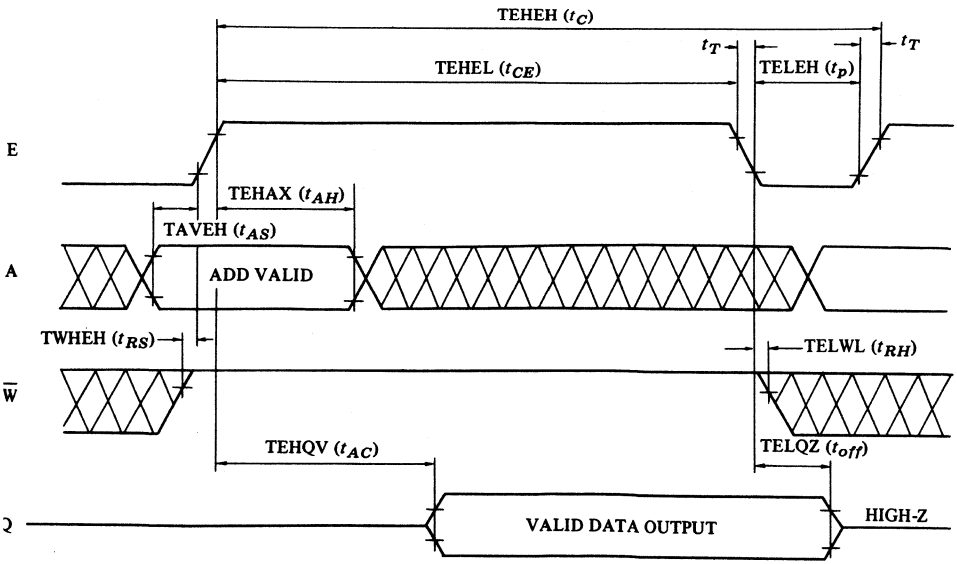
AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70℃)

- **AC TEST CONDITIONS**

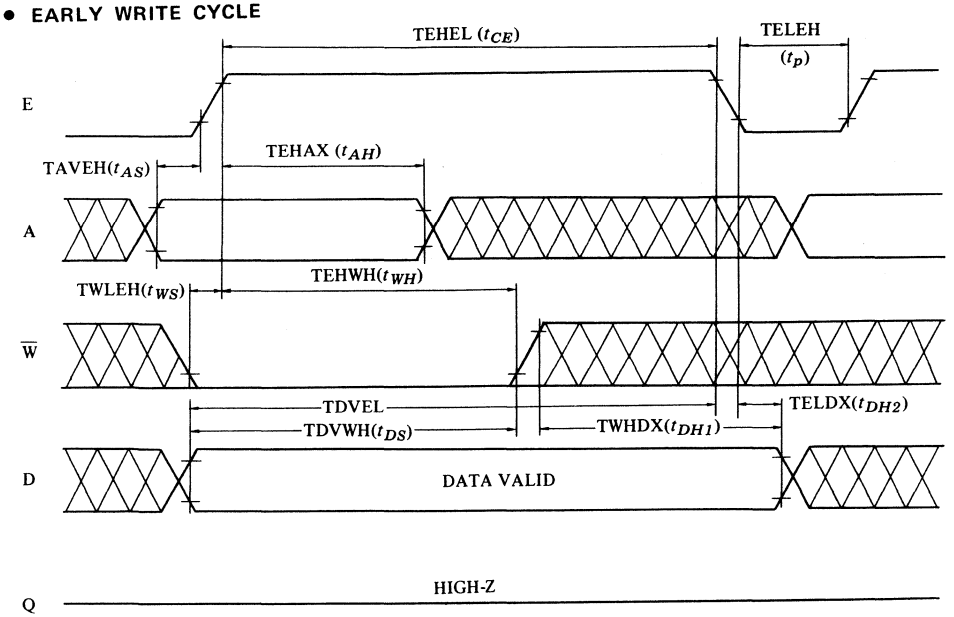
Input High Level 2.4V
Input Low Level 0.8V
Input Rise and Fall Times 20ns
Timing Measurement Levels 2.4V, 0.8V
Reference Level ..... V_{OH}=2.0V, V_{OL}=0.8V
Output Load ..... 1TTL+C_L=100pF

Item	Symbol	min.	max.	Unit
Read or Write Cycle Time	TEHEH (t_C)	640	—	ns
Random Access Time	TEHQV (t_{AC})	—	450	ns
Chip Enable Pulse Width	TEHEL (t_{CE})	450	—	ns
Chip Enable Precharge Time	TELEH (t_P)	150	—	ns
Address Hold Time	TEHAX (t_{AH})	200	—	ns
Address Setup Time	TAVEH (t_{AS})	20	—	ns
Output Buffer Turn-off Delay	TELQZ (t_{off})	0	100	ns
Write Enable Setup Time	TEHWL(t_{WS})	−20	—	ns
Data Input Hold Time	TWHDX(t_{DH1})	60	—	ns
Data Input Hold Time referenced to E	TELDX (t_{DH2})	40	—	ns
Write Enable Pulse Width	TWLWH(t_{WW})	120	—	ns
Chip Enable to Write Enable Delay*	TEHWL(t_{CWD})	350	—	ns
$\overline{W}$ to E Precharge Lead Time	TWLEL(t_{WPL})	150	—	ns
Data Input Setup Time	TDVWH, TDVEL(t_{DS})	100	—	ns
Write Enable Hold Time	TEHWH(t_{WH})	300	—	ns
Read Setup Time	TWHEH(t_{RS})	0	—	ns
Read Hold Time	TELWL(t_{RH})	0	—	ns
Chip Enable Rise/Fall Time	TT (t_T)	—	300	ns

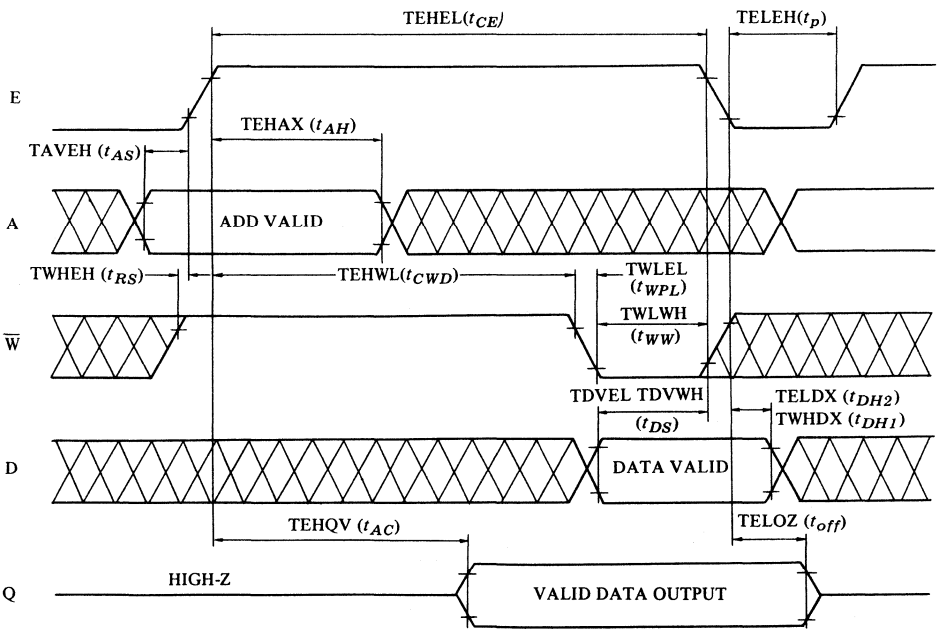
- **READ CYCLE**



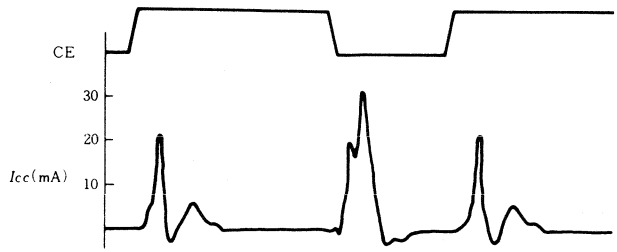
- **EARLY WRITE CYCLE**



- **READ MODIFY WRITE CYCLE AND READ WRITE CYCLE**

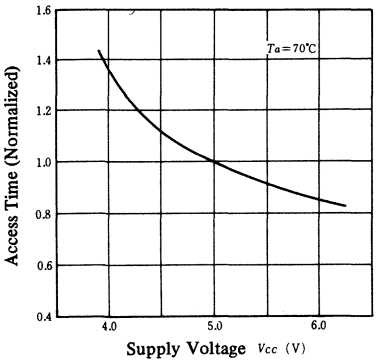


*For R-M-W Cycle (VALID DATA OUTPUT) $t_{CWD} \geqq 350$ ns, $t_{CE} \geqq 550$ ns
For R-W Cycle (INVALID DATA OUTPUT) 20 ns$< t_{CWD} <$ 350 ns, $t_{CE} \geqq 450$ ns

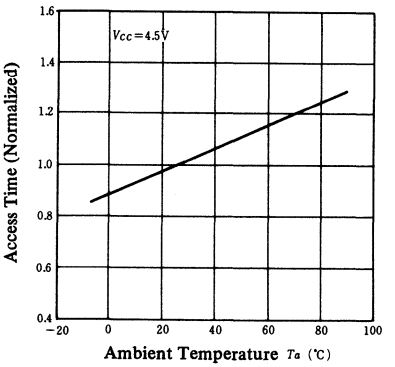


Notes: V_{CC} = 5.0V, Ta = 25°C

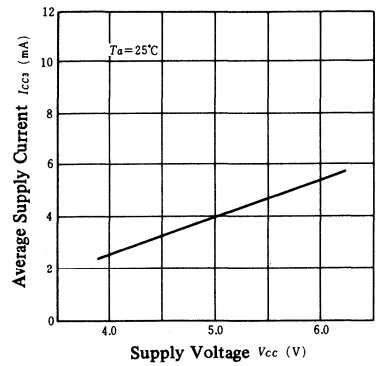
ACCESS TIME vs. SUPPLY VOLTAGE



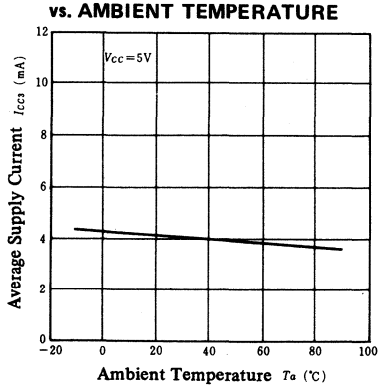
ACCESS TIME vs. AMBIENT TEMPERATURE



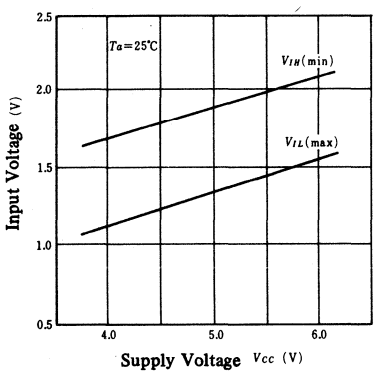
AVERAGE SUPPLY CURRENT vs. SUPPLY VOLTAGE



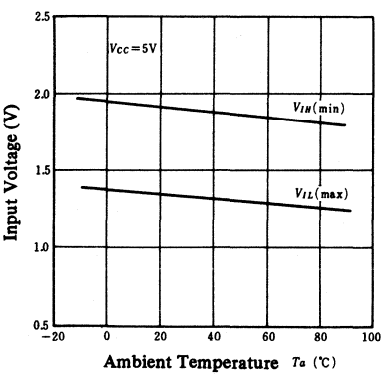
AVERAGE SUPPLY CURRENT vs. AMBIENT TEMPERATURE



INPUT VOLTAGE vs. SUPPLY VOLTAGE



INPUT VOLTAGE vs. AMBIENT TEMPERATURE



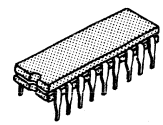
HM6147, HM6147-3, HM6147P, HM6147P-3

4096-word×1-bit High Speed Static CMOS RAM

FEATURES

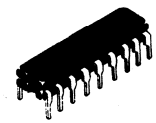
- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 55ns/70ns Max.
- Low Power Standby and Low Power Operation, Standby: 100 μW typ., Operation: 75mW typ.
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Pin-out Compatible with Intel 2147 NMOS STATIC RAM

HM6147, HM6147-3



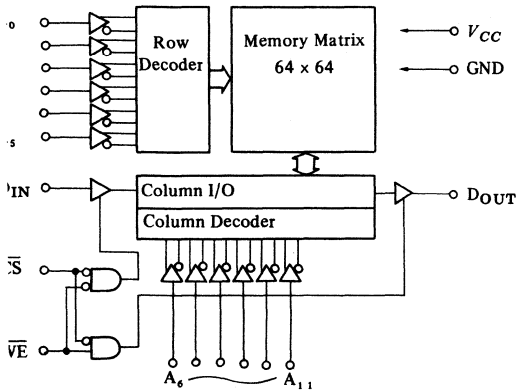
(DG-18)

HM6147P, HM6147P-3

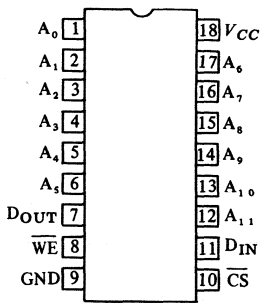


(DP-18)

BLOCK DIAGRAM



PIN ARRANGEMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND	V_{IN}	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C

RECOMMENDED DC OPERATING CONDITIONS ($0℃ \leqq Ta \leqq 70℃$)

Parameter	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	GND	0	0	0	V
Input High(logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input Low(logic 0) Voltage	V_{IL}	−0.3	—	0.8	V

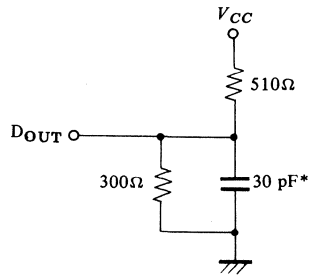
■ DC AND OPERATING CHARACTERISTICS ($0℃ \leqq Ta \leqq 70℃$, $V_{CC}=5V \pm 5\%$, GND=0V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit	Notes
Input Leakage Current	$\|I_{LI}\|$	$V_{CC}=5.25V$, GND to V_{CC}	—	—	2.0	μA	
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$, $V_{out}=0 \sim V_{CC}$	—	—	2.0	μA	
Operating Power Supply Current(1) DC	I_{CC}	$\overline{CS}=V_{IL}$, Output open	—	15	35	mA	
Operating Power Supply Current(2) DC	I_{CC1}	$\overline{CS}=V_{IL}$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	—	12	—	mA	[2]
Average Operating Current(3)	I_{CC2}	Cycle 150ns, duty 50%	—	14	—	mA	[2]
Standby Power Supply Current(1) DC	I_{SB}	$\overline{CS}=V_{IH}$	—	5	12	mA	
Standby Power Supply Current(2) DC	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	—	20	800	μA	
Output Low Voltage	V_{OL}	$I_{OL}=12mA$	—	—	0.40	V	
Output High Voltage	V_{OH}	$I_{OH}=-8.0mA$	2.4	—	—	V	

Notes: 1. Typical limits are at $V_{CC}=5.0V$, $Ta=25°C$ and specified loading.
2. Reference only

■ AC TEST CONDITIONS

- Input pulse levels: GND to 3.5V
- Input rise and fall times: 10 ns
- Input and output timing reference levels: 1.5V
- Output load: See Figure 1



*Including scope & jig capacitance
Figure 1 Output Load

■ CAPACITANCE ($Ta=25℃$, $f=1.0MHz$)[3]

Item	Symbol	Conditions	max.	Unit
Input Capacitance	C_{in}	$V_{in}=0V$	5	pF
Output Capacitance	C_{out}	$V_{out}=0V$	7	pF

Note 3: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS

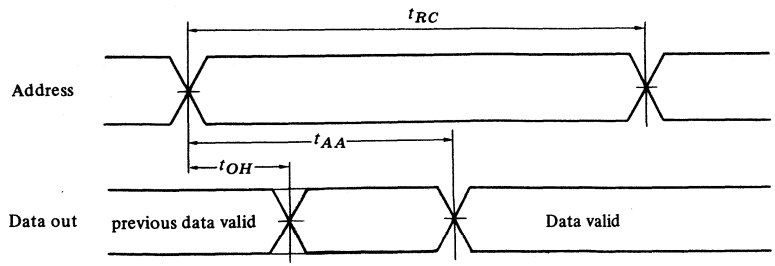
• **READ CYCLE** (Ta=0℃ to 70℃, V_{CC}=+5V±5%, unless otherwise noted.)

Parameter	Symbol	HM6147-3		HM6147		Unit
		min.	max.	min.	max.	
Read Cycle Time	t_{RC}	55	—	70	—	ns
Address Access Time	t_{AA}	—	55	—	70	ns
Chip Select Access Time	t_{ACS}	—	55	—	70	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns

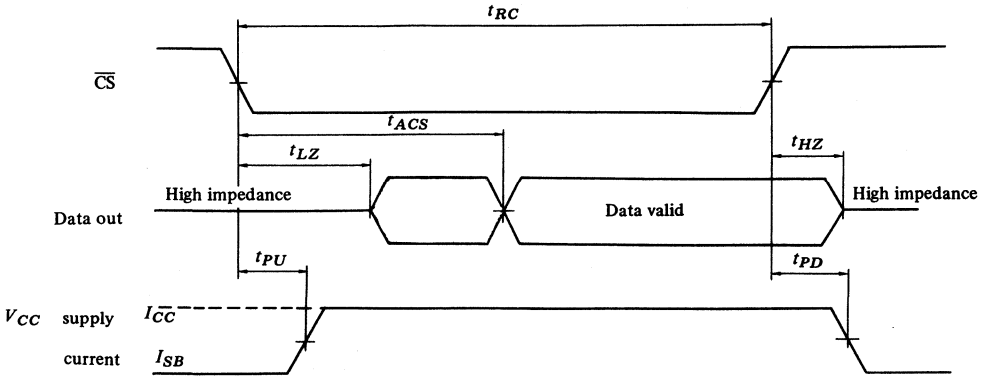
■ WRITE CYCLE

Parameter	Symbol	HM6147-3		HM6147		Unit
		min.	max.	min.	max.	
Write Cycle Time	t_{WC}	55	—	70	—	ns
Chip Selection to End of Write	t_{CW}	45	—	55	—	ns
Address Valid to End of Write	t_{AW}	45	—	55	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	35	—	40	—	ns
Write Recovery Time	t_{WR}	10	—	15	—	ns
Data Valid to End of Write	t_{DW}	25	—	30	—	ns
Data Hold Time	t_{DH}	10	—	10	—	ns
Write Enabled to Output in High Z	t_{WZ}	0	30	0	35	ns
Output Active from End of Write	t_{OW}	0	—	0	—	ns

■ TIMING WAVEFORM OF READ CYCLE NO. 1 [1] [2]

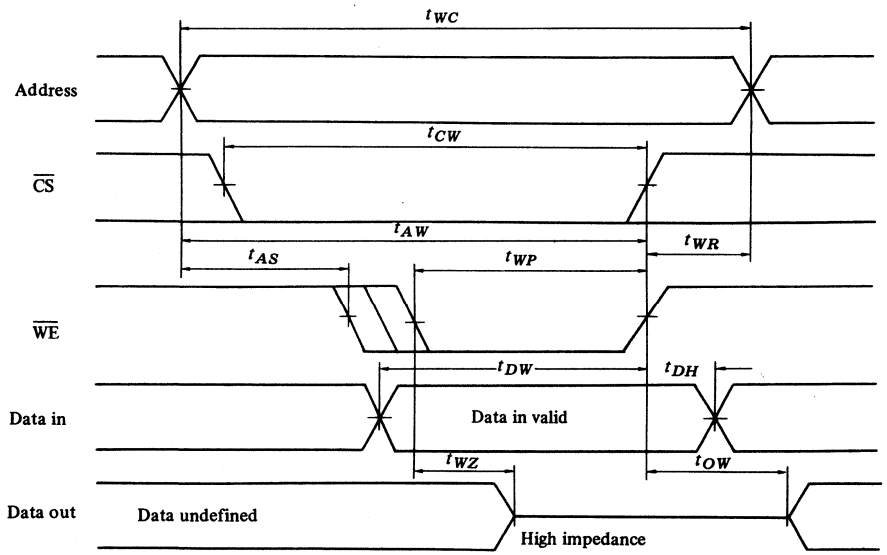


■ TIMING WAVEFORM OF READ CYCLE No. 2[1] [3]

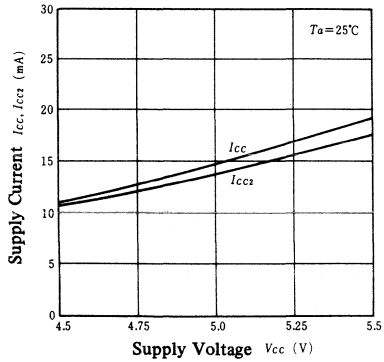


Notes: 1. $\overline{WE}$ is high for READ Cycle.
2. $\overline{CS}$ is low for READ Cycle.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

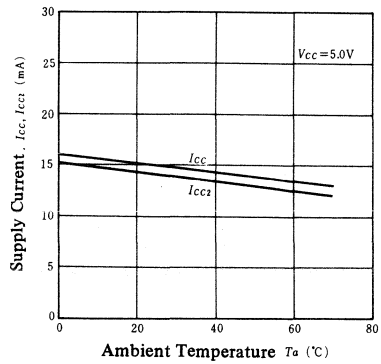
■ TIMING WAVEFORM OF WRITE CYCLE



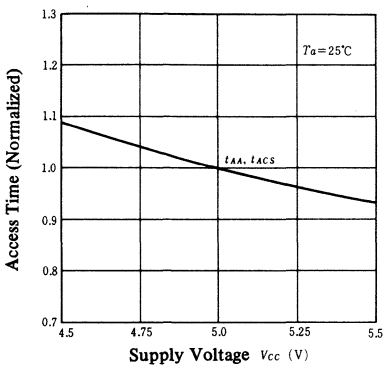
SUPPLY CURRENT vs. SUPPLY VOLTAGE



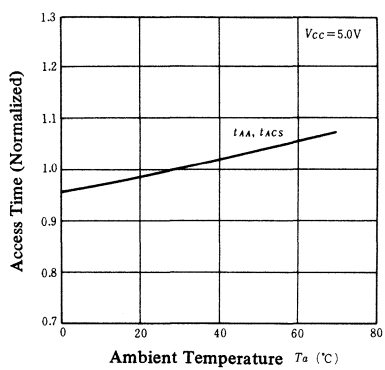
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



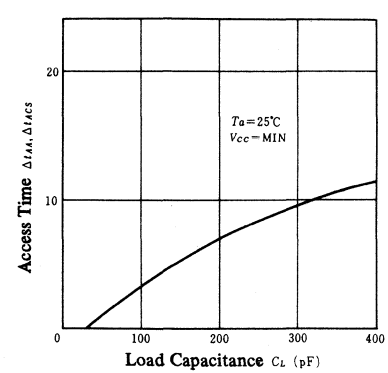
ACCESS TIME vs. SUPPLY VOLTAGE



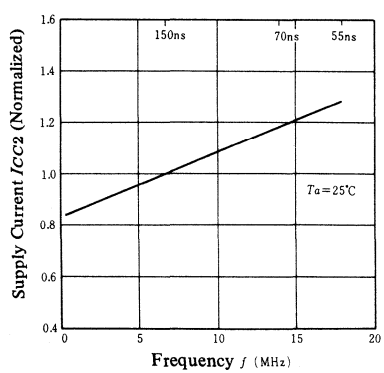
ACCESS TIME vs. AMBIENT TEMPERATURE



ACCESS TIME vs. LOAD CAPACITANCE



SUPPLY CURRENT vs. FREQUENCY

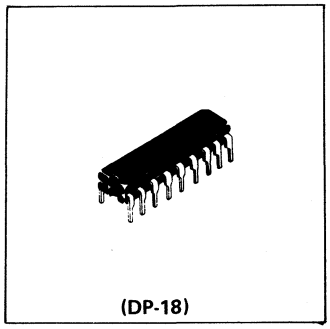


HM6147LP,HM6147LP-3

4096-word×1-bit High Speed Static CMOS RAM

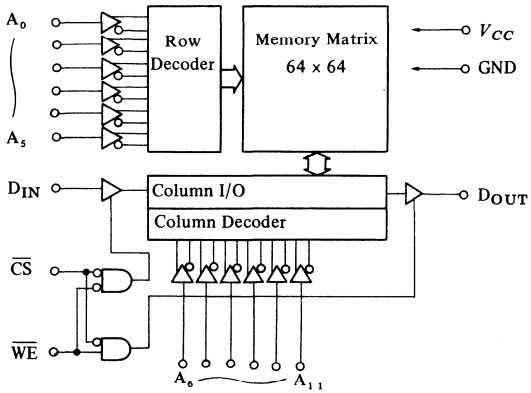
■ FEATURES

- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 55ns/70ns Max.
- Low Power Standby and Low Power Operation, Standby: 5μW typ., Operation: 75mW typ.
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Capability of Battery Back up Operation
- Pin-out Compatible with Intel 2147 NMOS STATIC RAM

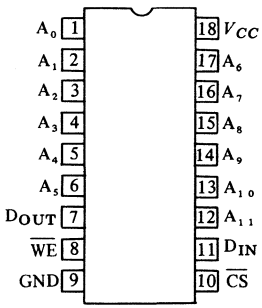


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND	V_{IN}	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq T_a \leqq 70°C$)

Parameter	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	GND	0	0	0	V
Input High(logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input Low(logic 0) Voltage	V_{IL}	−0.3	—	0.8	V

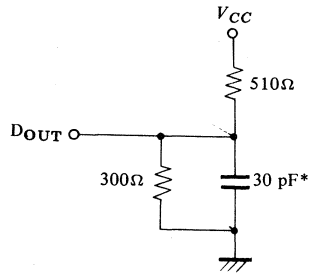
■ DC AND OPERATING CHARACTERISTICS ($0℃ \leqq Ta \leqq 70℃$, $V_{CC}=5V\pm5\%$, GND=0V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit	Notes
Input Leakage Current	$\lvert I_{LI} \rvert$	$V_{CC}=5.25V$, GND to V_{CC}	—	—	2.0	μA	
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{out}=0\sim V_{CC}$	—	—	2.0	μA	
Operating Power Supply Current(1) DC	I_{CC}	$\overline{CS}=V_{IL}$, Output open	—	15	35	mA	
Operating Power Supply Current(2) DC	I_{CC1}	$\overline{CS}=V_{IL}$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	—	12	—	mA	[2]
Average Operating Current(3)	I_{CC2}	Cycle 150ns, duty 50%	—	14	—	mA	[2]
Standby Power Supply Current(1) DC	I_{SB}	$\overline{CS}=V_{IH}$	—	5	12	mA	
Standby Power Supply Current(2) DC	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	—	1	100	μA	
Output Low Voltage	V_{OL}	$I_{OL}=12mA$	—	—	0.40	V	
Output High Voltage	V_{OH}	$I_{OH}=-8.0mA$	2.4	—	—	V	

Notes: 1. Typical limits are at $V_{CC}=5.0V$, $T_a=25°C$ and specified loading.
2. Reference only.

■ AC TEST CONDITIONS

- Input pulse levels: GND to 3.5V
- Input rise and fall times: 10 ns
- Input and output timing reference levels: 1.5V
- Output load: See Figure 1



*Including scope & jig capacitance
Figure 1 Output Load

■ CAPACITANCE ($Ta=25℃$, $f=1.0MHz$)[3]

Item	Symbol	Conditions	max.	Unit
Input Capacitance	C_{in}	$V_{IN}=0V$	5	pF
Output Capacitance	C_{out}	$V_{out}=0V$	7	pF

Note 3: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($Ta=0℃$ to $70℃$, $V_{CC}=5V\pm5\%$, unless otherwise noted.)

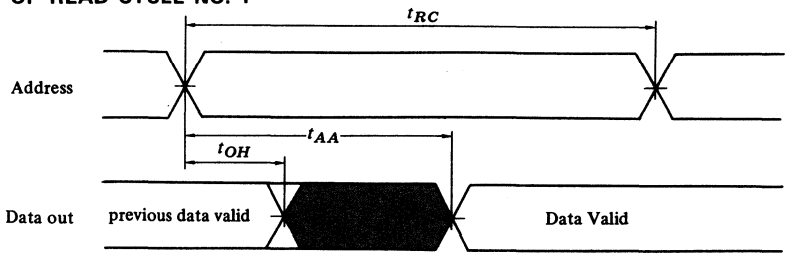
• READ CYCLE

Parameter	Symbol	HM6147LP-3		HM6147LP		Unit
		min.	max.	min.	max.	
Read Cycle Time	t_{RC}	55	—	70	—	ns
Address Access Time	t_{AA}	—	55	—	70	ns
Chip Select Access Time	t_{ACS}	—	55	—	70	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns

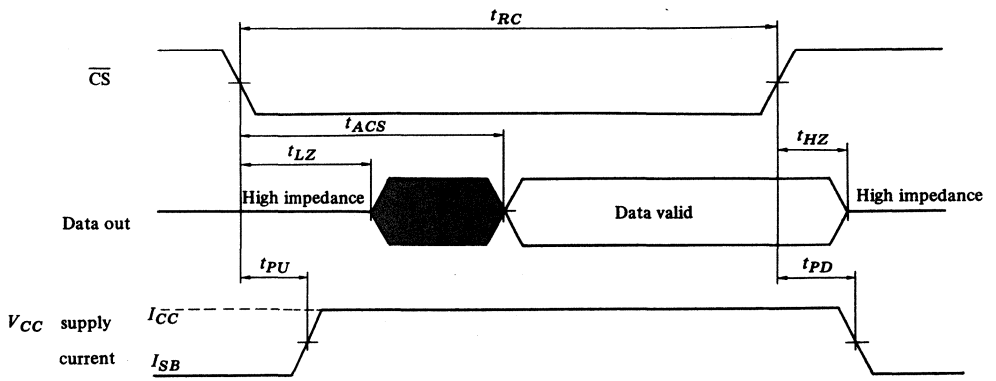
- **WRITE CYCLE**

Paramter	Symbol	HM6147LP-3		HM6147LP		Unit
		min.	max.	min.	max.	
Write Cycle Time	t_{WC}	55	—	70	—	ns
Chip Selection to End of Write	t_{CW}	45	—	55	—	ns
Address Valid to End of Write	t_{AW}	45	—	55	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	35	—	40	—	ns
Write Recovery Time	t_{WR}	10	—	15	—	ns
Data Valid to End of Write	t_{DW}	25	—	30	—	ns
Data Hold Time	t_{DH}	10	—	10	—	ns
Write Enabled to Output in High Z	t_{WZ}	0	30	0	35	ns
Output Active from End of Write	t_{OW}	0	—	0	—	ns

■ TIMING WAVEFORM OF READ CYCLE NO. 1 [1] [2]

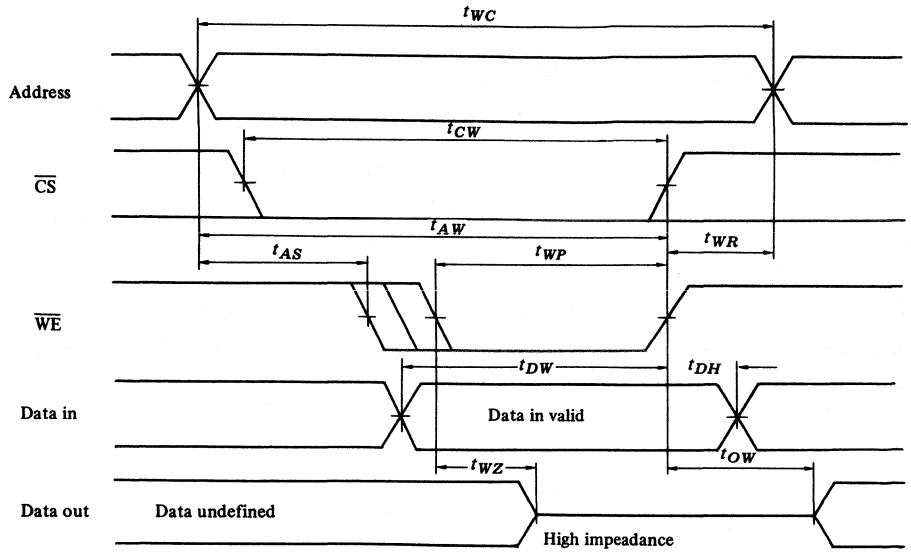


■ TIMING WAVEFORM OF READ CYCLE NO. 2 [1] [3]



Notes:
1. $\overline{WE}$ is high for READ Cycle.
2. $\overline{CS}$ is low for READ Cycle.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE

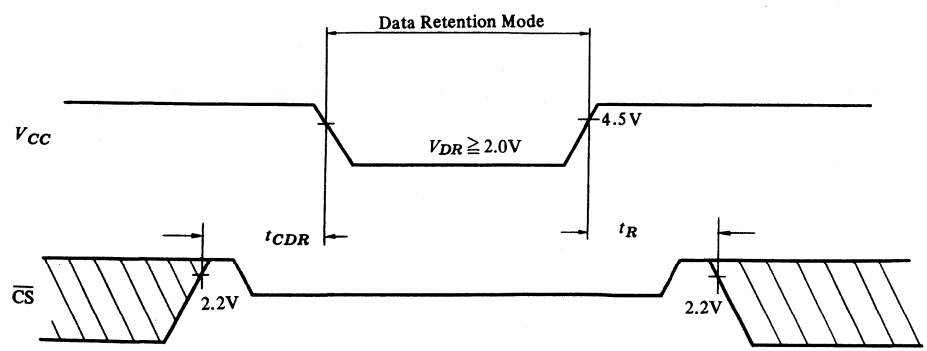


LOW V_{CC} RETENTION CHARACTERISTICS (Ta = 0°C to 70°C)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{in} \geqq V_{CC}-0.2V$ or $\leqq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}	V_{CC} = 2.0V, $\overline{CS} \geqq 1.8V$, $V_{in} \geqq 1.8V$ or $\leqq 0.2V$	—	—	40	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*	—	—	ns

t_{RC} = Read Cycle Time

LOW V_{CC} RETENTION CHARACTERISTICS

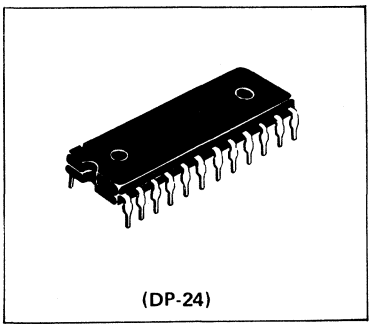


HM6116P-2, HM6116P-3, HM6116P-4

2048-word X 8-bit High Speed Static CMOS RAM

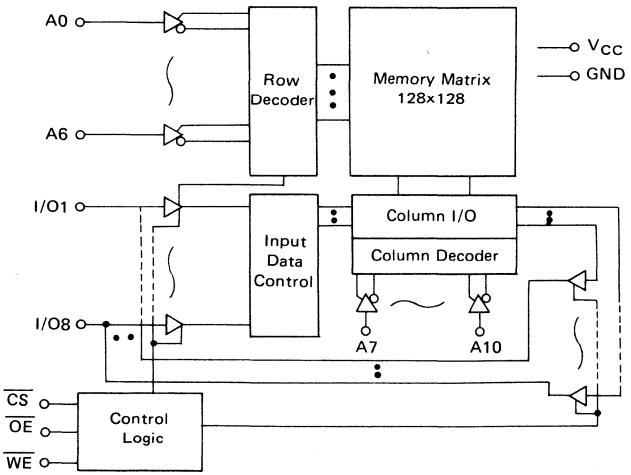
■ FEATURES

- Single 5V Supply and High Density 24 pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; Standby: 100μW (typ.)
  Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

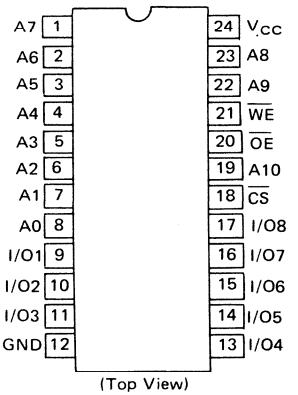


(DP-24)

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	−0.5 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1) ~ (3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−1.0*	–	0.8	V

Pulse Width: 50 ns, DC: V_{IL} min. = −0.3 V.

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5 V ±10%, GND = 0 V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	HM6116P-2			HM6116P-3/-4			Unit
			min.	typ.*	max.	min.	typ.*	max.	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = GND to V_{CC}	–	–	10	–	–	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	–	–	10	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	–	40	80	–	35	70	mA
	$I_{CC}1$**	V_{IH} = 3.5 V, V_{IL} = 0.6 V, $I_{I/O}$ = 0 mA	–	35	–	–	30	–	mA
Average Operating Current	$I_{CC}2$	Min. cycle, duty = 100%	–	40	80	–	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	–	5	15	–	5	15	mA
	$I_{SB}1$	$\overline{CS} \geqq V_{CC}$ −0.2V, $V_{in} \geqq V_{CC}$ −0.2V or $V_{in} \leqq$ 0.2V	–	0.02	2	–	0.02	2	mA
Output Voltage	V_{OL}	I_{OL} = 4 mA	–	–	0.4	–	–	–	V
		I_{OL} = 2.1 mA	–	–	–	–	–	0.4	
	V_{OH}	I_{OH} = −1.0 mA	2.4	–	–	2.4	–	–	V

*: V_{CC} = 5 V, T_a = 25°C
**: Reference Only

■ AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_a = 0 to +70°C)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4 V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5 V
Output Load: 1 TTL Gate and C_L = 100 pF (including scope and Jig)

● READ CYCLE

Item	Symbol	HM6116P-2		HM6116P-3		HM6116P-4		Unit
		min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	120	–	150	–	200	–	ns
Address Access Time	t_{AA}	–	120	–	150	–	200	ns
Chip Select Access Time	t_{ACS}	–	120	–	150	–	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	15	–	15	–	ns
Output Enable to Output Valid	t_{OE}	–	80	–	100	–	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	15	–	15	–	ns
Chip deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	–	15	–	15	–	ns

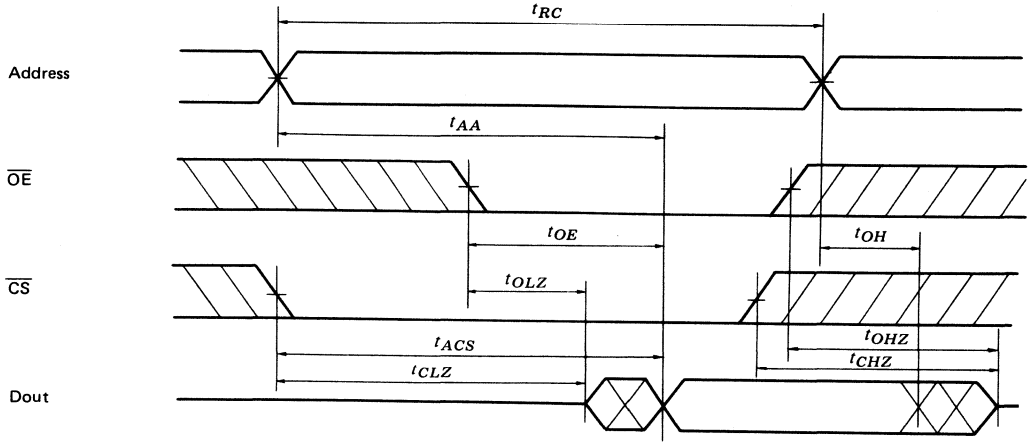
● WRITE CYCLE

Item	Symbol	HM6116P-2		HM6116P-3		HM6116P-4		Unit
		min.	typ.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	120	–	150	–	200	–	ns
Chip Selection to End of Write	t_{CW}	70	–	90	–	120	–	ns
Address Valid to End of Write	t_{AW}	105	–	120	–	140	–	ns
Address Set Up Time	t_{AS}	20	–	20	–	20	–	ns
Write Pulse Width	t_{WP}	70	–	90	–	120	–	ns
Write Recovery Time	t_{WR}	5	–	10	–	10	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	–	40	–	60	–	ns
Data Hold from Write Time	t_{DH}	5	–	10	–	10	–	ns
Output Active from End of Write	t_{OW}	5	–	10	–	10	–	ns

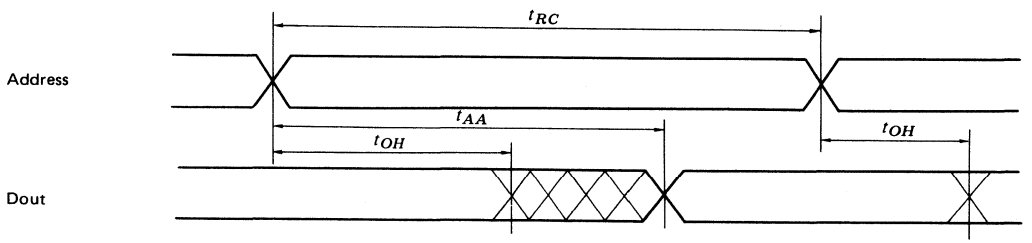
■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Conditions	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	7	pF

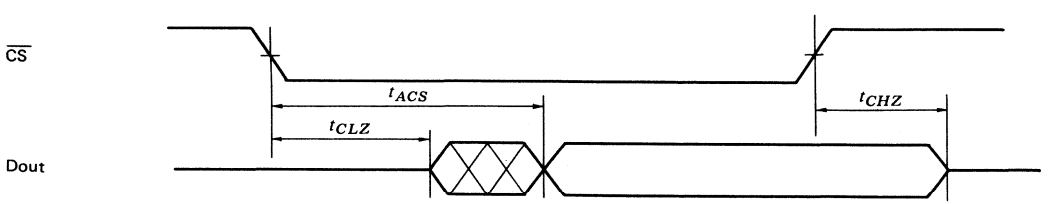
● Read Cycle (1) Notes) 1, 5



● Read Cycle (2) Notes) 1, 2, 4, 5



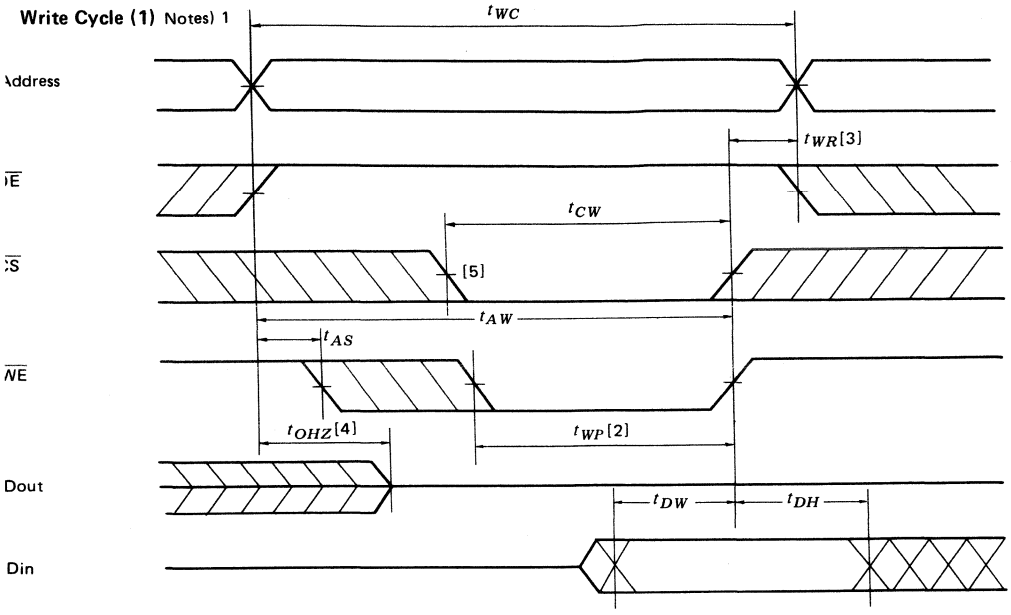
● Read Cycle (3) Notes) 1, 3, 4, 5



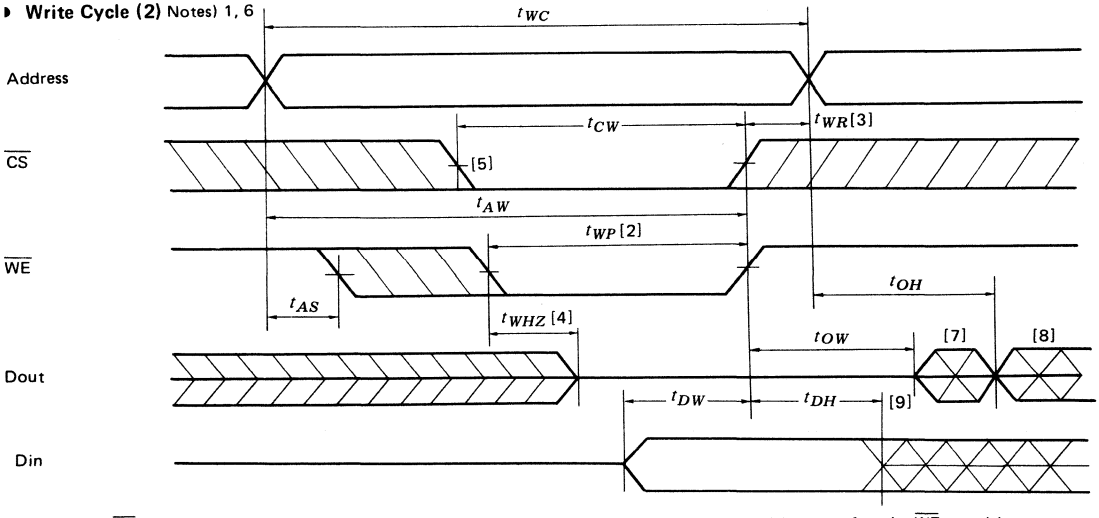
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.
5. When $\overline{CS}$ is Low, the address input must not be in the high impedance state.

TIMING WAVEFORM

Write Cycle (1) Notes) 1

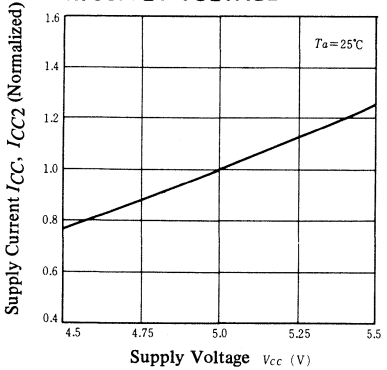


Write Cycle (2) Notes) 1, 6

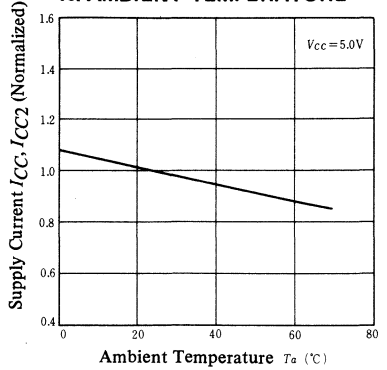


NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
7. D_{out} is the same phase of write data of this write cycle.
8. D_{out} is the read data of next address.
9. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

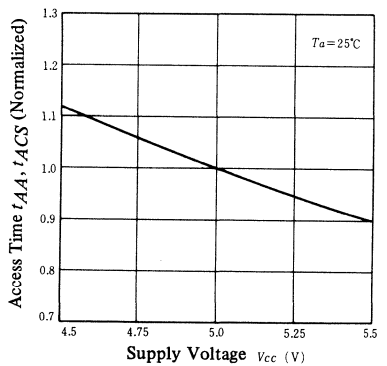
SUPPLY CURRENT vs. SUPPLY VOLTAGE



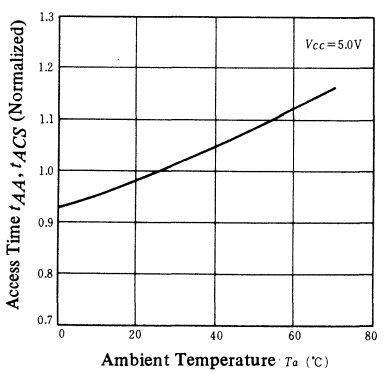
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



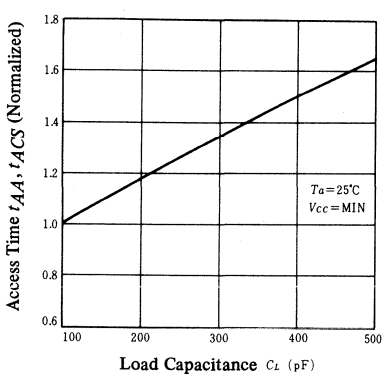
ACCESS TIME vs. SUPPLY VOLTAGE



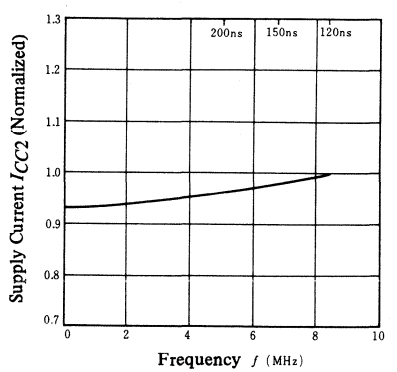
ACCESS TIME vs. AMBIENT TEMPERATURE



ACCESS TIME vs. LOAD CAPACITANCE



SUPPLY CURRENT vs. FREQUENCY

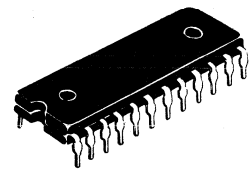


HM6116LP-2, HM6116LP-3, HM6116LP-4

2048-word X 8-bit High Speed Static CMOS RAM

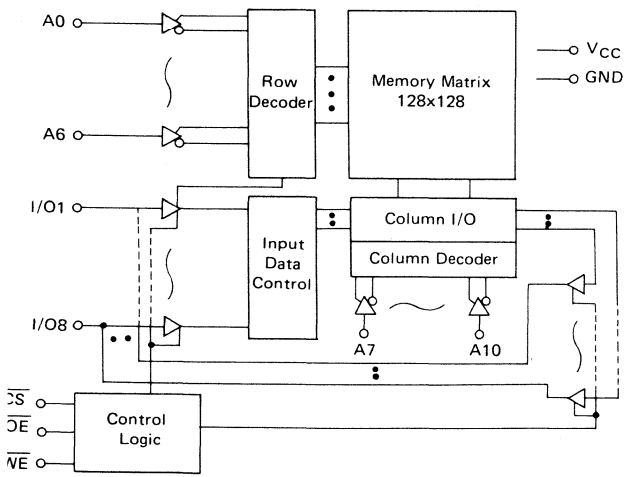
FEATURES

- Single 5V Supply and High Density 24 pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; Standby: 20μW (typ.)
  Operation: 160mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

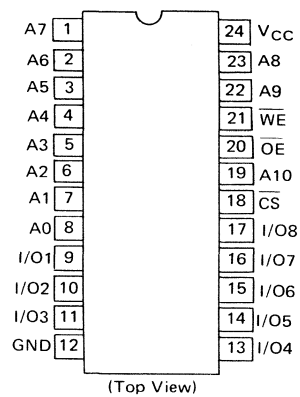


(DP-24)

FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	−0.5 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−1.0*	–	0.8	V

* Pulse Width: 50 ns, DC: V_{IL} min. = −0.3V.

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	HM6116LP-2			HM6116LP-3/-4			Unit
			min.	typ.*	max.	min.	typ.*	max.	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = GND to V_{CC}	–	–	2	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	–	–	2	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	–	35	70	–	30	60	mA
	I_{CC1}**	V_{IH} = 3.5V, V_{IL} = 0.6V, $I_{I/O}$ = 0mA	–	30	–	–	25	–	mA
Average Operating Current	I_{CC2}	Min. cycle, duty = 100%	–	35	70	–	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	–	4	12	–	4	12	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC} −0.2V, V_{in} ≧ V_{CC} −0.2V or V_{in} ≦ 0.2V	–	4	100	–	4	100	μA
Output Voltage	V_{OL}	I_{OL} = 4mA	–	–	0.4	–	–	–	V
		I_{OL} = 2.1mA	–	–	–	–	–	0.4	
	V_{OH}	I_{OH} = −1.0mA	2.4	–	–	2.4	–	–	V

*: V_{CC} = 5V, T_a = 25°C
**: Reference Only

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF
(including scope and Jig)

• READ CYCLE

Item	Symbol	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit
		min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	120	–	150	–	200	–	ns
Address Access Time	t_{AA}	–	120	–	150	–	200	ns
Chip Select Access Time	t_{ACS}	–	120	–	150	–	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	15	–	15	–	ns
Output Enable to Output Valid	t_{OE}	–	80	–	100	–	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	15	–	15	–	ns
Chip deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	–	15	–	15	–	ns

WRITE CYCLE

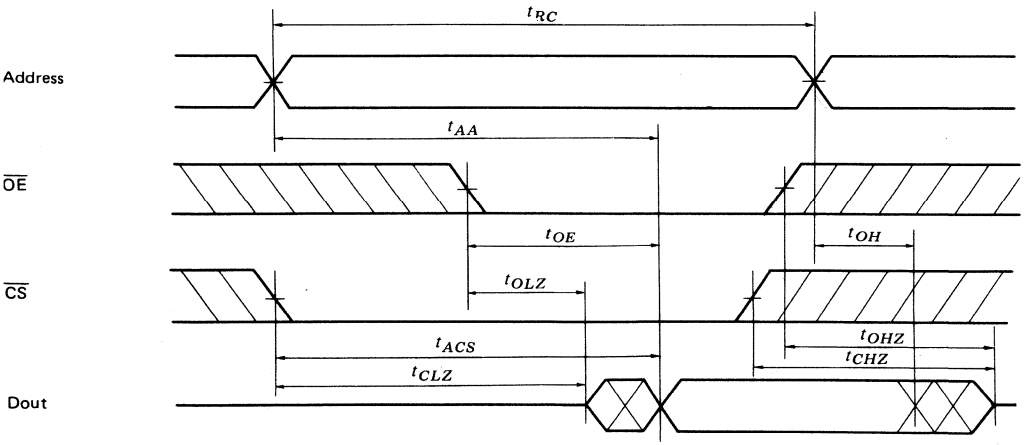
Item	Symbol	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit
		min.	typ.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	120	–	150	–	200	–	ns
Chip Selection to End of Write	t_{CW}	70	–	90	–	120	–	ns
Address Valid to End of Write	t_{AW}	105	–	120	–	140	–	ns
Address Set Up Time	t_{AS}	20	–	20	–	20	–	ns
Write Pulse Width	t_{WP}	70	–	90	–	120	–	ns
Write Recovery Time	t_{WR}	5	–	10	–	10	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	–	40	–	60	–	ns
Data Hold from Write Time	t_{DH}	5	–	10	–	10	–	ns
Output Active from End of Write	t_{OW}	5	–	10	–	10	–	ns

CAPACITANCE (f = 1MHz, T_a = 25°C)

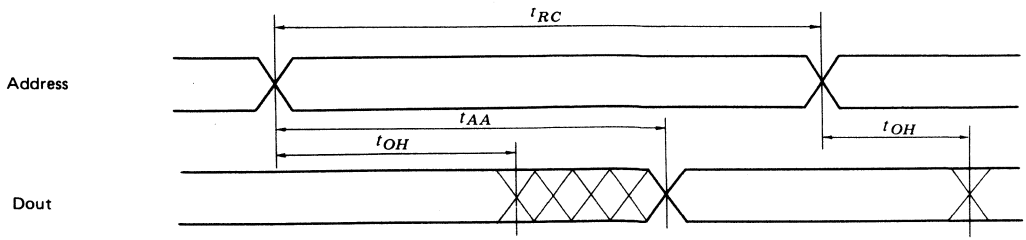
Item	Symbol	Test Conditions	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	7	pF

TIMING WAVEFORM

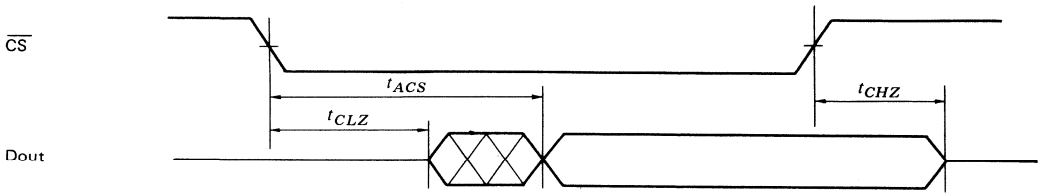
- **Read Cycle (1)** Notes) 1, 5



- **Read Cycle (2)** Notes) 1, 2, 4, 5

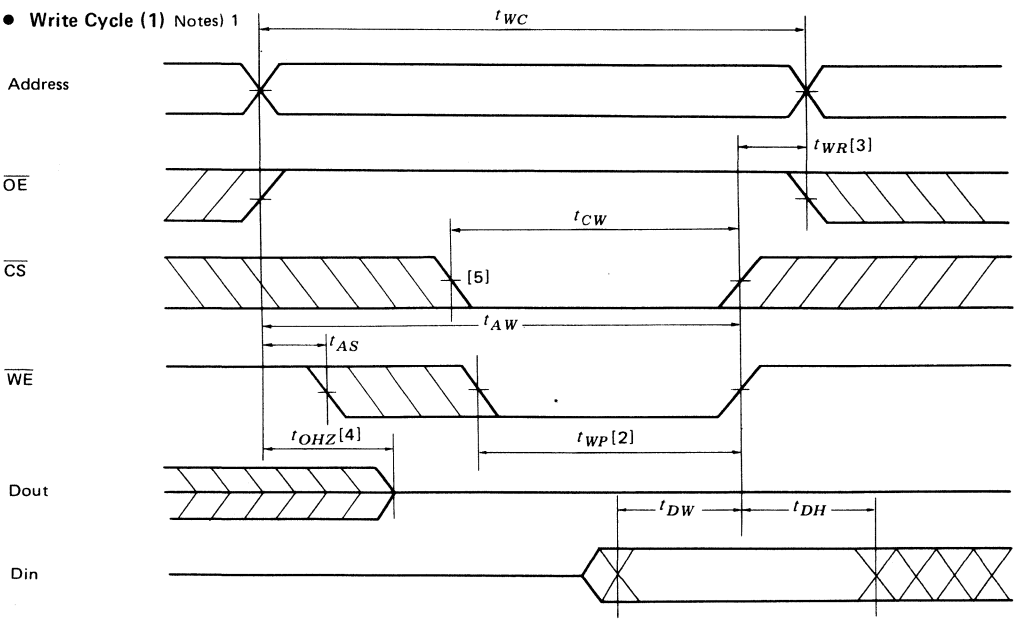


- **Read Cycle (3)** Notes) 1, 3, 4, 5

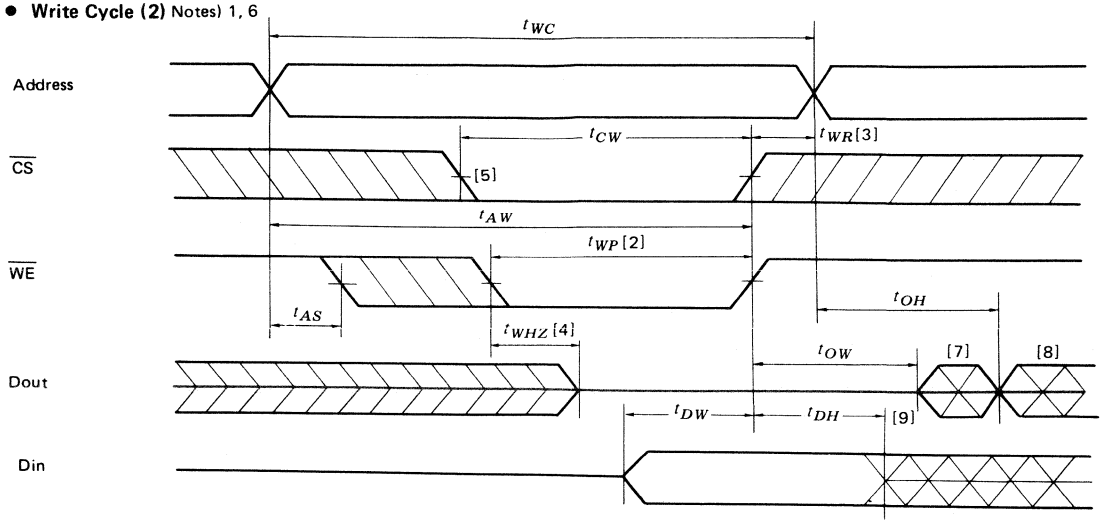


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.
5. When $\overline{CS}$ is Low, the address input must not be in the high impedance state.

- **Write Cycle (1)** Notes) 1



● **Write Cycle (2)** Notes) 1, 6



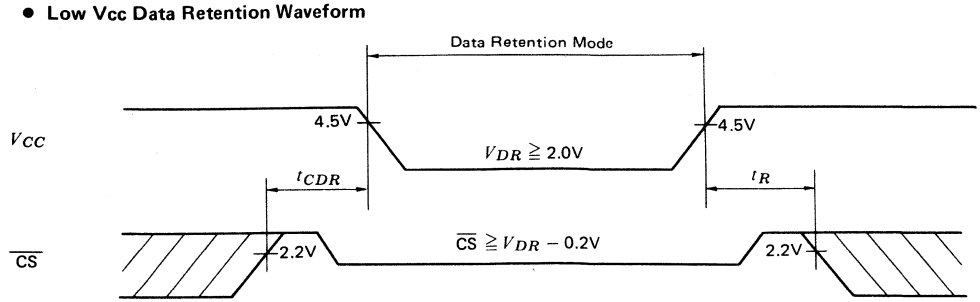
NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
7. D_{out} is the same phase of write data of this write cycle.
8. D_{out} is the read data of next address.
9. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC} - 0.2V$ $V_{IN} \geqq V_{CC} - 0.2V$ or $V_{IN} \leqq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS} \geqq 2.8V$ $V_{IN} \geqq 2.8V$ or $V_{IN} \leqq 0.2V$	–	–	50	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		* t_{RC}	–	–	ns

* t_{RC} = Read Cycle Time.

● **Low V_{CC} Data Retention Waveform**



MOS DYNAMIC RAM

HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4, HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4

16384-word × 1-bit Dynamic Random Access Memory

The HM4716A is a 16,384 word by 1 bit MOS random access memory circuit fabricated with HITACHI's double poly N-channel silicon gate process for high performance and high functional density. The HM4716A uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation. Multiplexed address inputs permit the HM4716A to be packaged in a standard 16 pin DIP on 0.3 inch centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The HM4716A is designed to facilitate upgrading of the 16-pin 4K RAM. However, the data output latch incorporated in the present 4K design is not appropriate for 16K RAM's. This new generation of memory products (16K RAM's) requires a slightly modified output stage to allow more system flexibility. Instead of the conventional latch, the HM4716A output is controlled by the Column Address Storobe ($\overline{CE}$). Data out of the HM4716A will remain valid from the access time from the Column Address Strobe unitl $\overline{CE}$ goes into precharge (logic 1). However, in early write cyles ($\overline{W}$ active low before $\overline{CE}$ goes low), the data output will remain in the high impedance (open-circuit) state throughout the entire cycle. This type of output operation results in some very significant system implications.

1. Common I/O Operation

If all write operation are handled in the "early write" mode, then data in can be connected directly to data-out on a printed circuit board.

2. Data Output Control

Data well remain valid at the output during a read cycle from TCELQV until $\overline{CE}$ returns to precharge.

This allows data to be valid from one cycle up until a new memory cycle begins.

3. Two Methods of Chip Selection

Both $\overline{CE}$ and/or $\overline{RE}$ can be decoded for chip selection.

4. Refresh

Refreshing can be accomplished every 2ms by either of the two following methods:

(1) normal read or write cycles on 128 addresses, A0 to A6.

(2) $\overline{RE}$ only cycles on 128 addresses, A0 to A6.

A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

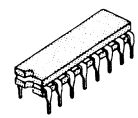
$\overline{RE}$ only regreshes results in a substantial reduction in operating power.

5. Page Mode Operation

The HM4716A is designed for page mode operation.

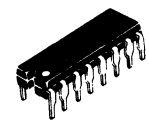
Old	New	Definitions
A0-A6	A0-A6	Address Inputs
$\overline{CAS}$	$\overline{CE}$	Column Address Strobe
D_{IN}	D	Data In
D_{OUT}	Q	Data Out
$\overline{RAS}$	$\overline{RE}$	Row Address Strobe
$\overline{WRITE}$	$\overline{W}$	Read/Write Input
V_{BB}	VBB	Power (−5V)
V_{CC}	VCC	Power (+5V)
V_{DD}	VDD	Power (+12V)
V_{SS}	VSS	Ground

HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4



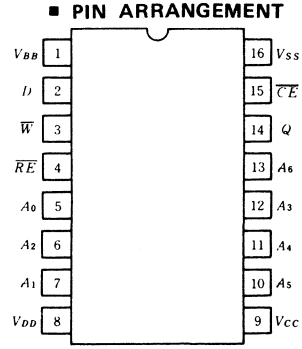
(DG-16A)

HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4



(DP-16)

■ **PIN ARRANGEMENT**



(Top View)

HITACHI

■ FEATURES

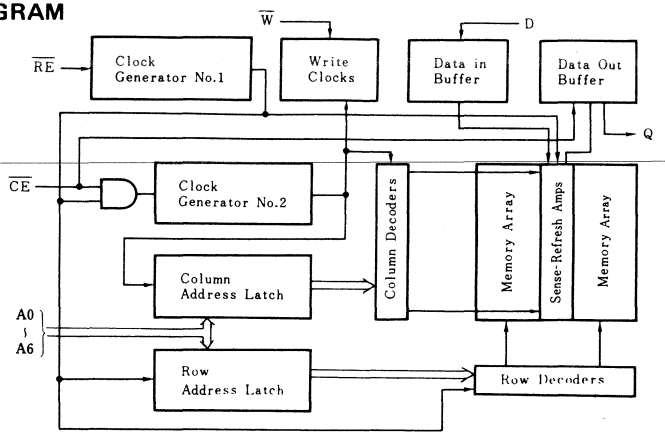
- All Inputs Including Clocks TTL Compatible
- Input Latches for Address and Data in
- Three-State TTL Compatible Output
- Common I/O Capability
- Only 128 Refresh Cycles Required Every 2ms
- Standard Power Supplies +12V, +5V, −5V (all with 10% tolelance)
- Maximum Access Time

HM4716A-1	120ns
HM4716A-2	150ns
HM4716A-3	200ns
HM4716A-4	250ns

- Read or Write Cycle Time

HM4716A-1	320ns
HM4716A-2	320ns
HM4716A-3	375ns
HM4716A-4	410ns

■ FUNCTIONAL DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to VBB	−0.5V to+20V
Voltage on VDD, VCC Supplies relative to VSS	−0.5V to +15V
Voltage on Q pin relative to VSS	−0.5V to +10V
Operating Temperature, TA (Ambient)	0°C to +70°C
Storage Temperature (Ambient)*	−65°C to +150°C
Short-circuit output current	50mA
Power dissipation	1W

* In case of HM4716AP Series are −55°C to +125°C.

■ RECOMMENDED DC OPERATING CONDITIONS (TA = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	VDD	10.8	12.0	13.2	V	1
	VCC	4.5	5.0	5.5	V	
	VSS	0	0	0	V	
	VBB	−4.5	−5.0	−5.5	V	
Input High (logic 1) Voltage RE, CE, W	VIHC	2.7	—	6.5	V	1
Input High (logic 1) Voltage All inputs except RE, CE, W	VIH	2.4	—	6.5	V	1
Input Low (logic 0) Voltage all inputs	VIL	−1.0	—	0.8	V	1

■ DC ELECTRICAL CHARACTERISTICS (TA=0 to +70°C, VDD=12V±10%, VCC=5V±10%, VBB=−5V±10%, VSS=0V)

Parameter	Symbol	min.	max.	Units	Notes
OPERATING CURRENT	IDD1	—	35	mA	2
Average Power Supply Operating Current	ICC1	—	—	mA	3
($\overline{RE}$, $\overline{CE}$ Cycling; TRELREL=375ns)	IBB1	—	300	μA	2
STANDBY CURRENT	IDD2	—	1.5	mA	
Power Supply Standby Current ($\overline{RE}$ = $\overline{CE}$ = VIHC)	ICC2	−10	10	μA	5
	IBB2	—	100	μA	
REFRESH CURRENT	IDD3	—	27	mA	2
Average Power Supply Current, Refresh Mode	ICC3	−10	10	μA	5
($\overline{RE}$ Cycling, $\overline{CE}$=VIHC; TRELREL=375ns)	IBB3	—	300	μA	2
PAGE MODE CURRENT	IDD4	—	27	mA	
Average Power Supply Current, Page-mode Operation	ICC4	—	—	mA	3
($\overline{RE}$=VIL, $\overline{CE}$ Cycling; TCELCEL=225ns)	IBB4	—	300	μA	
INPUT LEAKAGE Input Leakage Current, any Input (VBB=−5V, VIN=0 to +7V, all other pins not under test=0V)	IIL	−10	10	μA	
OUTPUT LEAKAGE Output Leakage Current (Q is Disabled, VOUT=0 to +5.5V)	IOL	−10	10	μA	5
OUTPUT LEVELS Output High (Logic 1) Voltage (IOUT=−5mA)	VOH	2.4	VCC	V	4
Output Low (Logic 0) Voltage (IOUT=4.2mA)	VOL	0	0.4	V	

NOTES

1. All voltages referenced to VSS, VBB must be applied before and removed after other supply voltage.
2. Current depend on cycle rate: maximum current is measured at the fastest cycle rate.
3. ICC depends upon output loading. The VCC supply is connected to the output buffer only.
4. Output voltage will swing from VSS to VCC when activated with no current loading. For purposes of maintaining data in standby mode, VCC may be reduced to VSS without affecting refresh operations or data retention. However, the VOH (min) specification is not guaranteed in this mode.
5. ICC2, ICC3 and IOL consists of leakage current only.
6. AC measurements assume TT = 5ns.
7. VIHC (min) or VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also, transition times are measured between VIHC or VIH and VIL.
8. Assumes that TRELCEL = TRELCEL (max). If TRELCEL is greater than the maximum recommended value shown in this table, TRELQV exceeds the value shown.
9. Assumes that TRELCEL = TRELCEL (max).
10. Measured with a load circuit equivalent to 2TTL loads and 100pF (in case of HM4716A-2:1 TTL and 50pF). And VSS + 0.8V, VSS + 2.0V are the reference level for measuring timing of Q.
11. TCEHQZ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation with the TRELCEL (max) limit insures that TRELQC (max) can be met TRELCEL (max) is specified as a reference point only; if TRELCEL is greater than the specified TRELCEL (max) limit, then access time is controlled exclusively by TCELQV.
13. These parameters are referenced to $\overline{CE}$ leading edge in early write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.
14. TWLCEL, TCELWL and TRELWL are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if TWLCEL = TWLCEL (min), the cycle is an early write and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if TCELWL = TCELWL (min) and TRELWL will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
15. Capacitance measured with Boonton Meter or effective capacitance measuring method.
16. $\overline{CE}$ = VIHC to disable Q.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

TA=0 to +70°C, VDD=12V±10%, VCC=5V±10%, VSS=0V, VBB=−5V±10%)

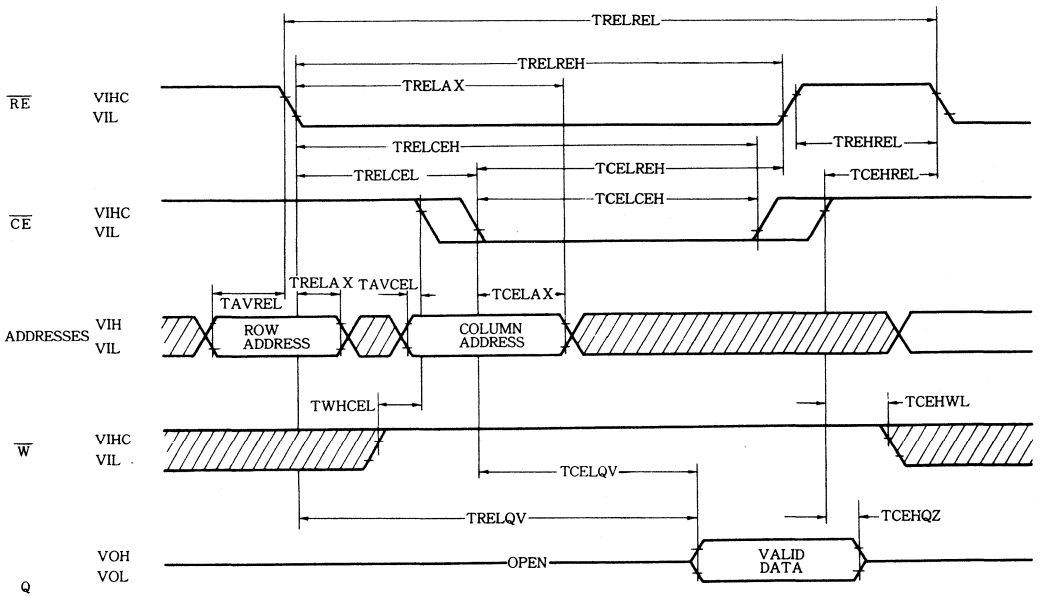
Parameter	Symbol		HM4716A-1		HM4716A-2		HM4716A-3		HM4716A-4		Units	Notes
	Old	New	min.	max.	min.	max.	min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	TRELREL	320	–	320	–	375	–	410	–	ns	
Read-Write Cycle Time	t_{RWC}	TRELREL	320	–	320	–	375	–	515	–	ns	
Page Mode Cycle Time	t_{PC}	TCELCEL	160	–	170	–	225	–	275	–	ns	
Access Time From $\overline{RE}$	t_{RAC}	TRELQV	–	120	–	150	–	200	–	250	ns	8, 10
Access Time From $\overline{CE}$	t_{CAC}	TCELQV	–	80	–	100	–	135	–	165	ns	9, 10
Output Buffer Turn-off Delay	t_{OFF}	TCEHQZ	0	35	0	50	0	60	0	70	ns	11
Transition Time (Rise and Fall)	t_T	TT	3	35	3	35	3	50	3	50	ns	7
$\overline{RE}$ Precharge Time	t_{RP}	TREHREL	100	–	100	–	120	–	150	–	ns	
$\overline{RE}$ Pulse Width	t_{RAS}	TRELREH	120	10000	150	10000	200	10000	250	10000	ns	
$\overline{RE}$ Hold Time	t_{RSH}	TCELREH	80	–	100	–	135	–	165	–	ns	
$\overline{CE}$ Pulse Width	t_{CAS}	TCELCEH	80	10000	100	10000	135	10000	165	10000	ns	
$\overline{CE}$ Hold Time	t_{CSH}	TRELCEH	120	–	150	–	200	–	250	–	ns	
$\overline{RE}$ to $\overline{CE}$ Delay Time	t_{RCD}	TRELCEL	15	40	25	50	30	65	40	85	ns	12
CE to RE Precharge Time	t_{CRP}	TCEHREL	0	–	−20	–	−20	–	−20	–	ns	
Row Address Set-up Time	t_{ASR}	TAVREL	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	TRELAX	15	–	20	–	25	–	35	–	ns	
Column Address Set-up Time	t_{ASC}	TAVCEL	−5	–	−5	–	−5	–	−5	–	ns	
Column Address Hold Time	t_{CAH}	TCELAX	40	–	45	–	55	–	75	–	ns	
Column Address Hold Time Reference to $\overline{RE}$	t_{AR}	TRELAX	80	–	95	–	120	–	160	–	ns	
Read Command Set-up Time	t_{RCS}	TWHCEL	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	TCEHWL	0	–	20	–	20	–	20	–	ns	
Write Command Hold Time	t_{WCH}	TCELWH	40	–	45	–	55	–	75	–	ns	
Write Command Hold Time Referenced $\overline{RE}$	t_{WCR}	TRELWH	80	–	95	–	120	–	160	–	ns	
Write Command Pulse Width	t_{WP}	TWLWH	40	–	45	–	55	–	75	–	ns	
Write Command to $\overline{RE}$ Lead Time	t_{RWL}	TWLREH	50	–	60	–	80	–	100	–	ns	
Write Command to $\overline{CE}$ Lead Time	t_{CWL}	TWLCEH	50	–	60	–	80	–	100	–	ns	
Data-in Set-up Time	t_{DS}	TDVCEL	0	–	0	–	0	–	0	–	ns	13
Data-in Hold Time	t_{DH}	TCELDX	40	–	45	–	55	–	75	–	ns	13
Data-in Hold Time Referenced $\overline{RE}$	t_{DHR}	TRELDX	80	–	95	–	120	–	160	–	ns	
$\overline{CE}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	TCEHCEL	60	–	60	–	80	–	100	–	ns	
Refresh Period	t_{REF}	TRVRV	–	2	–	2	–	2	–	2	ms	
$\overline{W}$ Command Set-up Time	t_{WCS}	TWLCEL	0	–	−20	–	−20	–	−20	–	ns	14
$\overline{CE}$ to $\overline{RE}$ Delay	t_{CWD}	TCELWL	60	–	70	–	95	–	125	–	ns	14
$\overline{RE}$ to $\overline{W}$ Delay	t_{RWD}	TRELWL	100	–	120	–	160	–	200	–	ns	14
$\overline{RE}$ Precharge to $\overline{CE}$ Hold Time	t_{RPC}	TREHCEL	0	–	0	–	0	–	0	–	ns	

AC ELECTRICAL CHARACTERISTICS

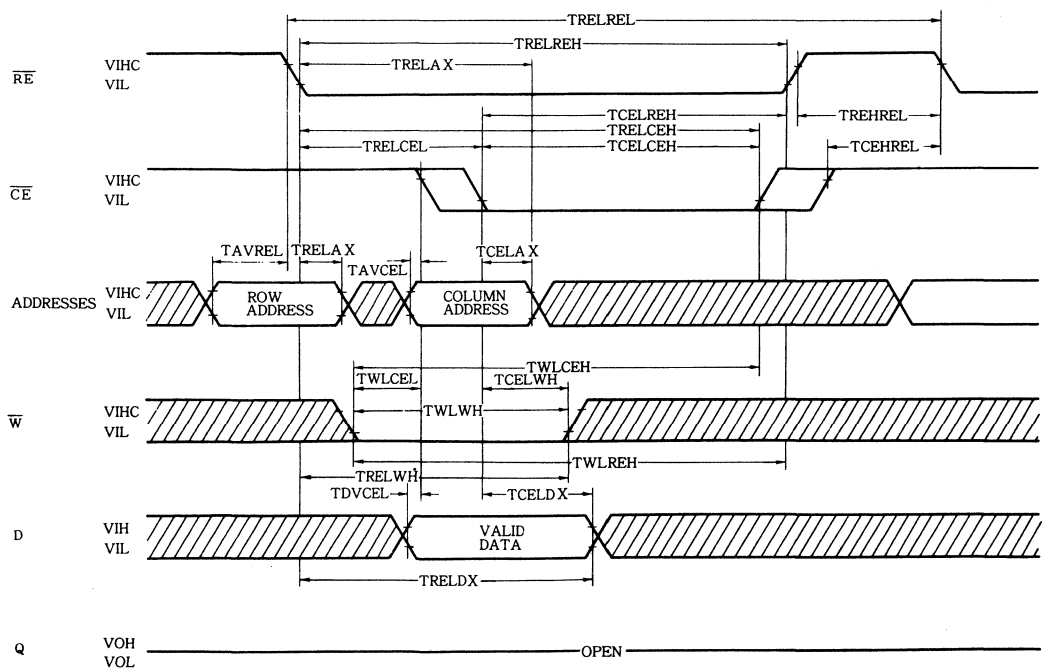
Parameter	Symbol	typ.	max.	Units	Notes
Input Capacitance (A0-A6, D)	CI1	—	5	pF	15
Input Capacitance $\overline{RE}$, $\overline{CE}$, $\overline{W}$	CI2	—	10	pF	15
Output Capacitance (Q)	CQ	—	7	pF	15, 16

■ TIMING WAVEFORMS

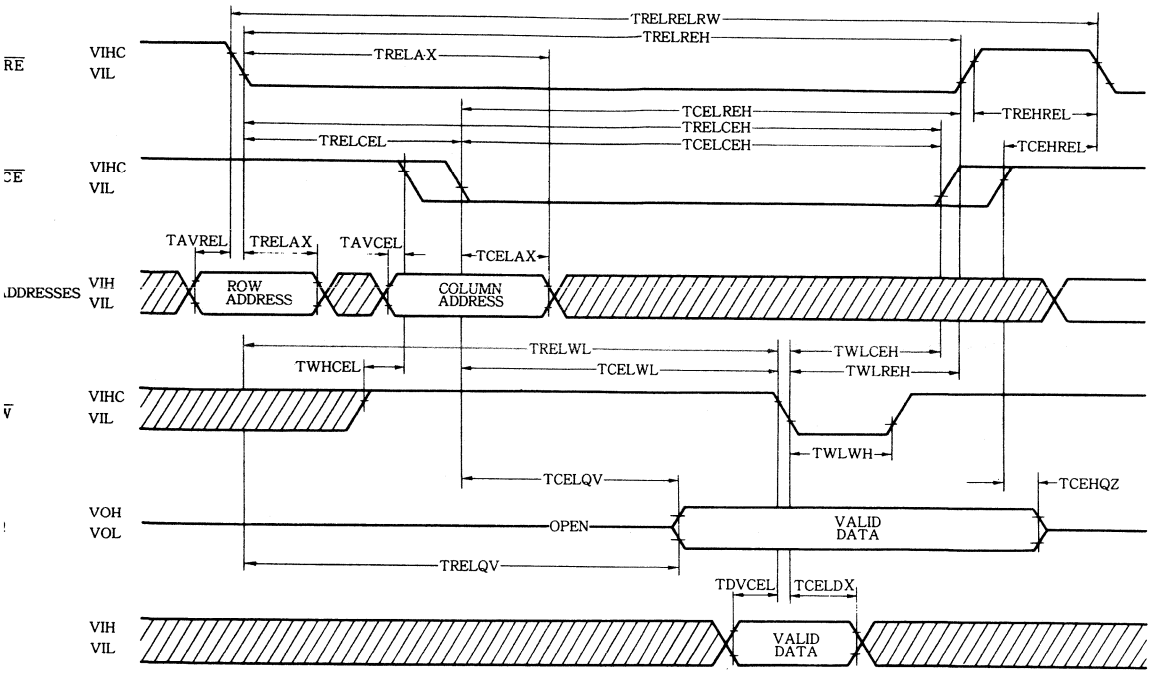
• READ CYCLE



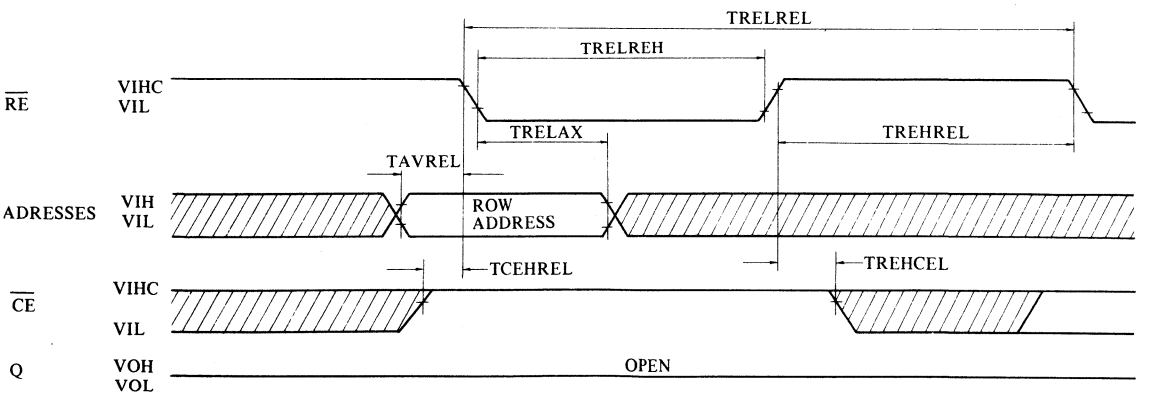
• WRITE CYCLE (EARLY WRITE)



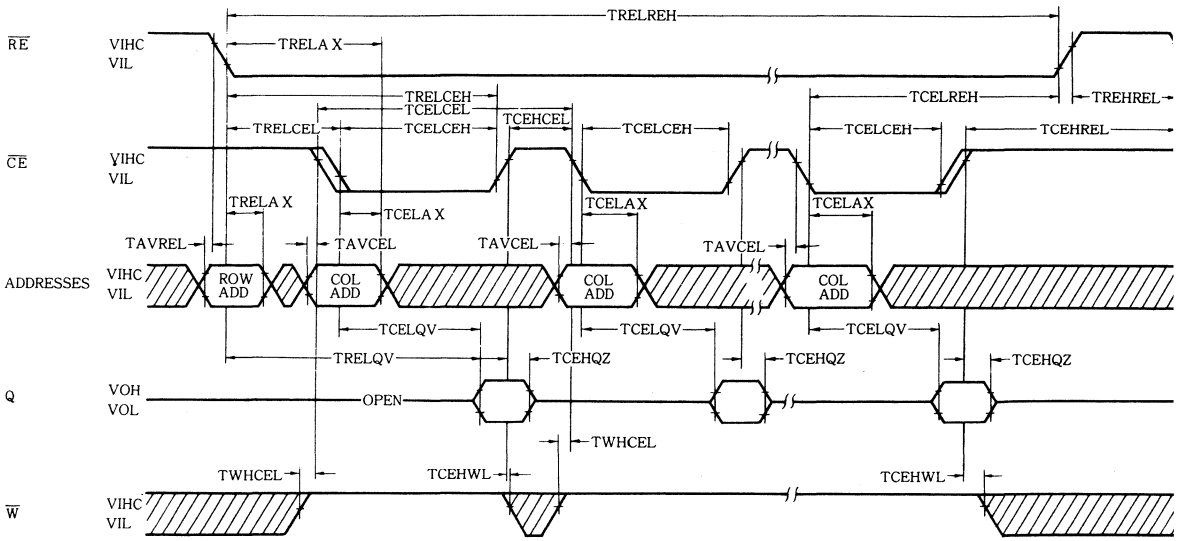
READ-WRITE/READ-MODIFY-WRITE CYCLE



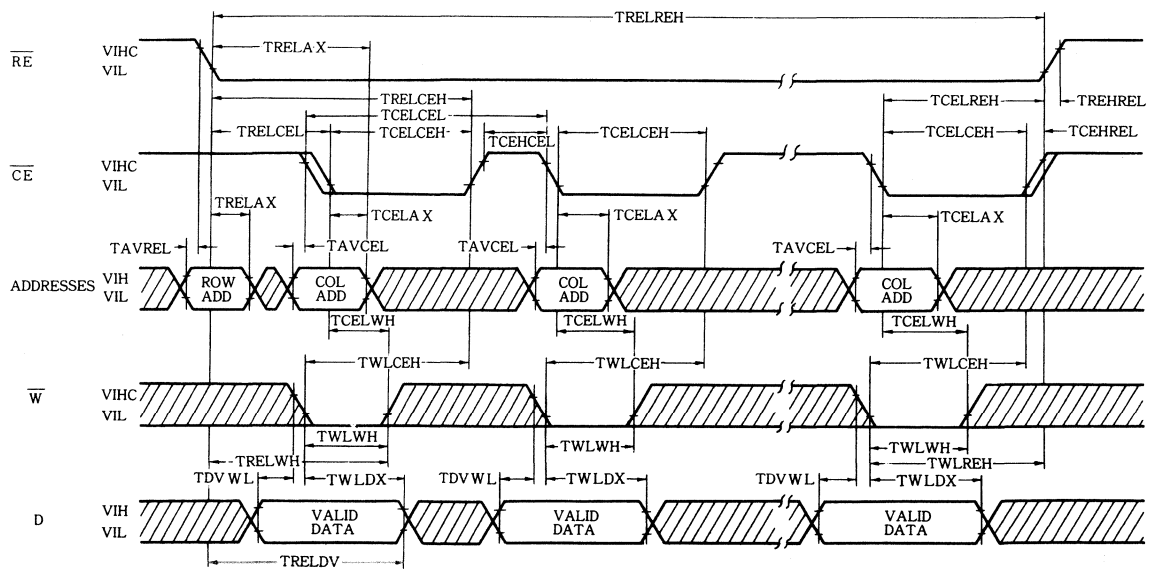
"$\overline{RE}$ ONLY" REFRESH CYCLE



- **PAGE MODE READ CYCLE**

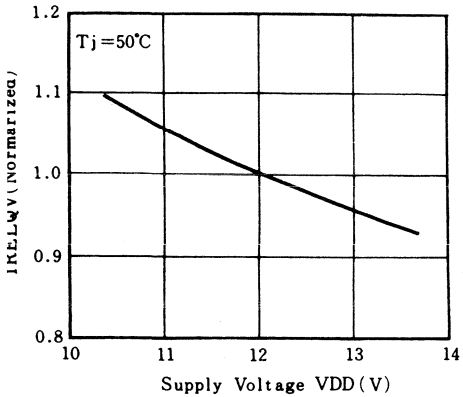


- **PAGE MODE WRITE CYCLE**

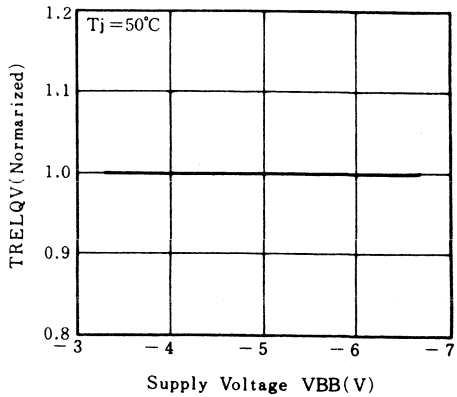


■ TYPICAL CHARACTERISTICS

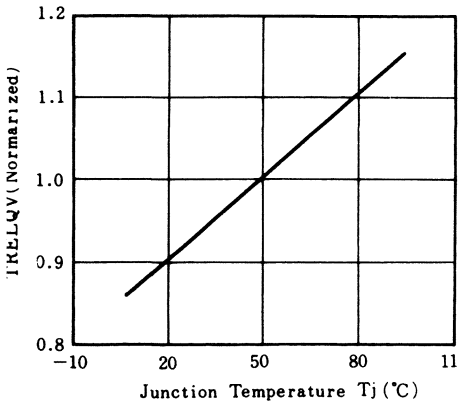
ACCESS TIME (NORMARIZED) vs. VDD



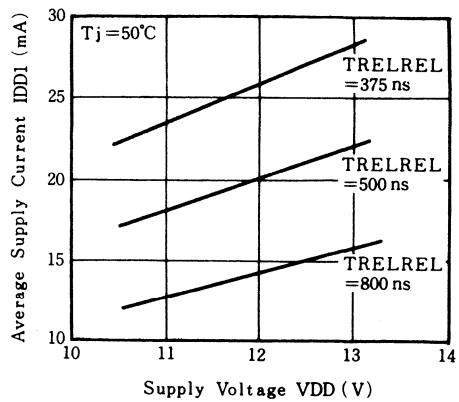
ACCESS TIME (NORMARIZED) vs. V_{BB}



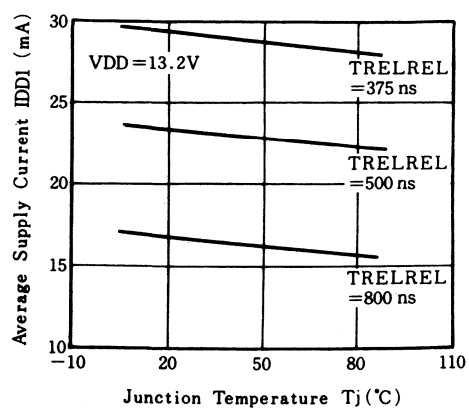
ACCESS TIME (NORMARIZED) vs. Tj



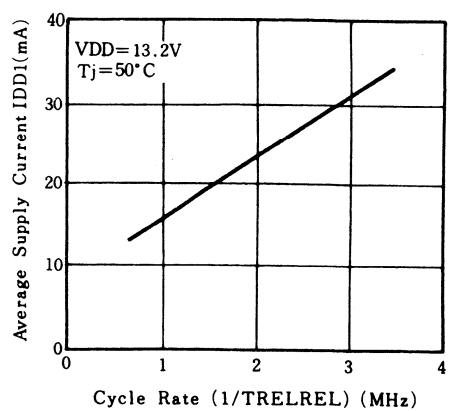
IDDI vs. V_{DD}



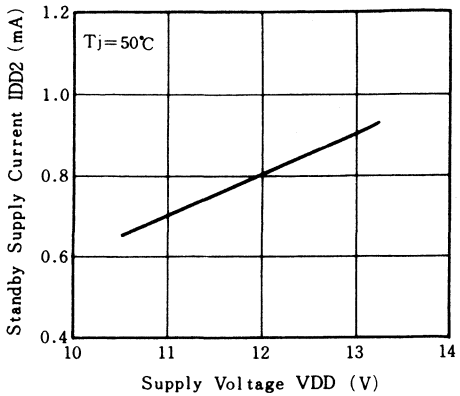
IDDI vs. Tj



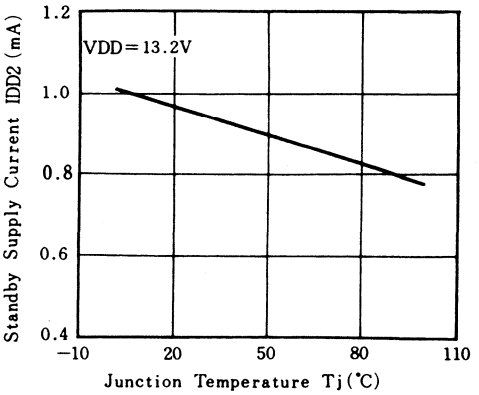
IDDI vs. CYCLE RATE



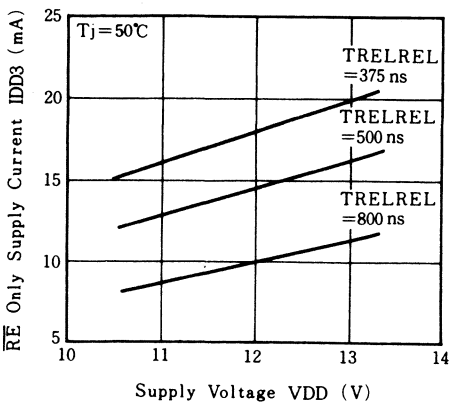
IDD2 (STANDBY) vs. VDD



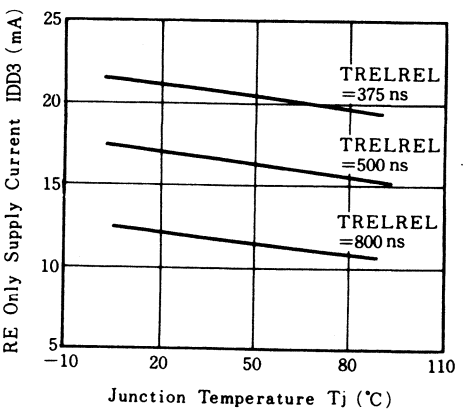
IDD2 (STANDBY) vs. Tj



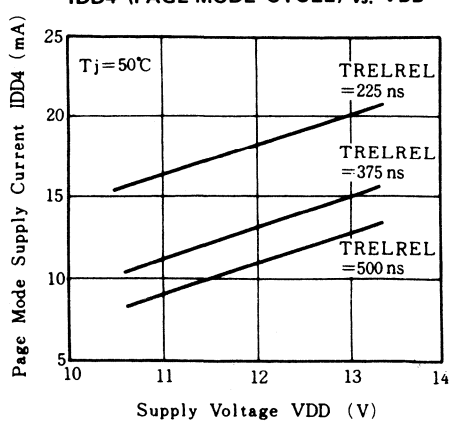
IDD3 ($\overline{RE}$ ONLY CYCLE) vs. VDD



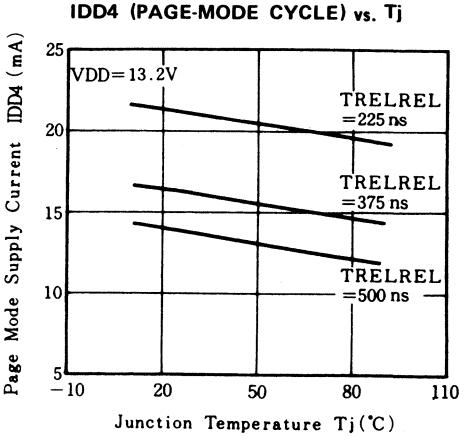
IDD3 ($\overline{RE}$ ONLY CYCLE) vs. Tj



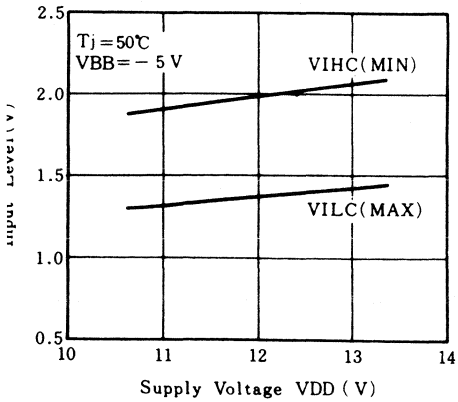
IDD4 (PAGE-MODE CYCLE) vs. VDD



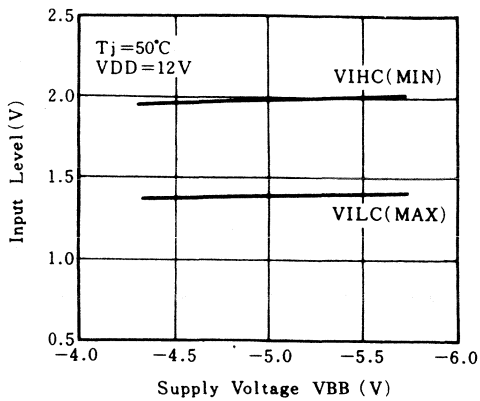
IDD4 (PAGE-MODE CYCLE) vs. Tj



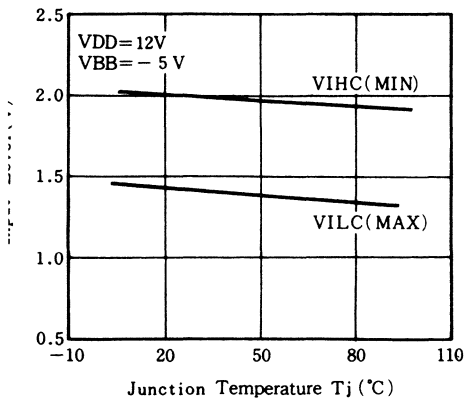
CLOCK INPUT LEVELS vs. VDD



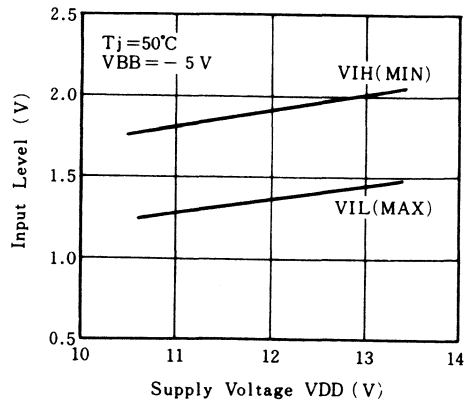
CLOCK INPUT LEVELS vs. V_{BB}



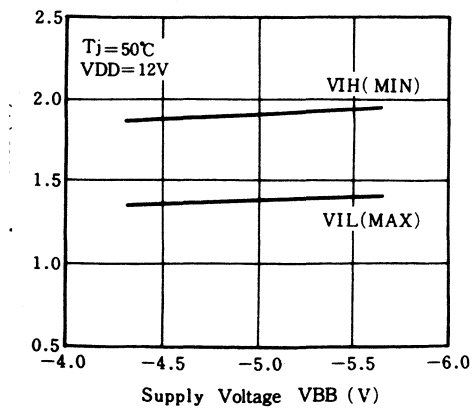
CLOCK INPUT LEVELS vs. Tj



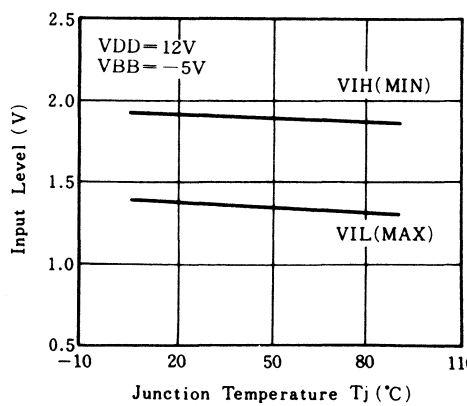
ADDRESS AND DATA INPUT LEVELS vs. V_{DD}



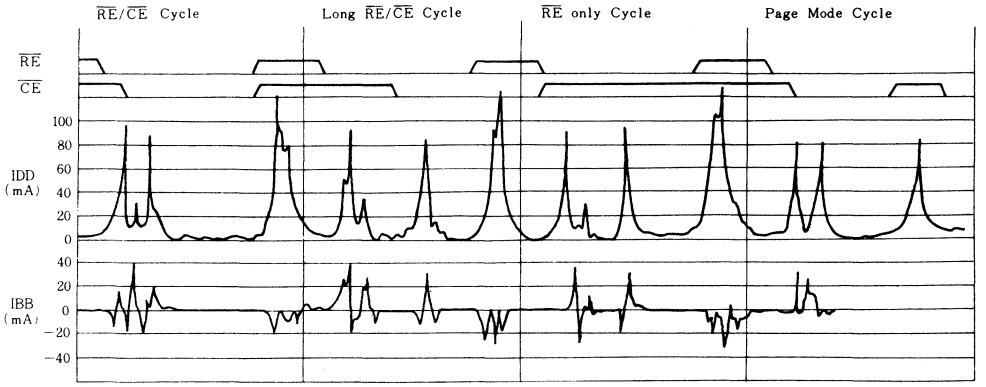
ADDRESS AND DATA INPUT LEVELS vs. V_{BB}



ADDRESS AND DATA INPUT LEVELS vs. Tj



■ CURRENT WAVEFORMS



NOTE : VDD = 13.2V, VBB = −4.5V, Ta = 25°C

APPLICATION INFORMATION

READ CYCLE;

A read cycle begins with addresses stable and a negative going transistion of $\overline{RE}$. The time delay between the stable address and the start of $\overline{RE}$-on is controlled by parameter TAVREL.
Following the time when $\overline{RE}$ reaches its low level, the row address must be held stable long enough to be captured.
This controlling parameter is TRELAX. Following this interval, the address can be changed from row address to column address.
When the column address is stable, $\overline{CE}$ can be turned on.
The leading edge of $\overline{CE}$ is controlled by parameter TRELCEL.
The basic limit on the $\overline{CE}$ leading edge is that $\overline{CE}$ cannot start intill the column address is stable, and this is controlled by parameter TAVCEL.
The column address must be held stable long enough to be captured.
The controlling parameter is TCELAX. Note that TRELCEL-max) is not an operating limit of the HM4716A though its specification is listed on the data sheets. If $\overline{CE}$ becomes on later than TRELCEL(max), the access time from $\overline{RE}$ will be increased by the time which TRELCEL exceeds TRELCEL-max).
Following the time when $\overline{CE}$ reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is TCELQV-access time from $\overline{CE}$. The access time from $\overline{RE}$-TRELQV-is the time from $\overline{RE}$-on to valid data. The minimum value of TRELQV is derived as the sum of TRELCEL(max) and TCELQV. The selected output data is held valid internally untill $\overline{CE}$ becomes high, and then Q pin becomes high impedance. This parameter is TCEHQZ.

WRITE CYCLE;

A write cycle is performed by bringing $\overline{W}$ low before or during $\overline{CE}$-on.
Two different write cycles can be defined as;
Write cycle – Write data are available at the beginning of the $\overline{CE}$-on so that the write operationstarts at the beginning. In this mode, D and $\overline{W}$ signal times are not in any critical path for determining cycle time
following the time when $\overline{W}$ reaches its low level. $\overline{W}$ must be held stable long enough to be captured. This $\overline{W}$-on pulse duration is called TWLWH.
The time required to capture write data in a latch is called WLDX.
This cycle is called an "early write"
Read Write cycle – This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated. $\overline{W}$ and D are delayed until after Q. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, D and $\overline{W}$ become critical path signals for determining cycle time.

• CLOCK-OFF TIMING;

$\overline{RE}$ and $\overline{CE}$ must stay on for Q stabilized to valid data. In the case of $\overline{CE}$, this is controlled by parameaer TCELCEH(min). In the case of $\overline{RE}$, this controlled by parameter TCELREH(min).
Following the end of $\overline{RE}$, $\overline{CE}$ must stay off long enough to precharge internal circuits. The only parameter of concern is TREHREL.
Normally $\overline{CE}$ is not required to be off for a minimum time of TCEHREL.
However, in a page mode memory operation, there is a TCEHCEL(min) specification to control the $\overline{CE}$-off time.

• DATA OUTPUT;

Q is three-state TTL compatible with a fan-out of two standard TTL loads.
When $\overline{CE}$ is high, Q is in a high impedance state. When $\overline{CE}$ is low, valid data appears after TCELQV at a read cycle, and Q is not valid at an early-write cycle.

• REFRESH;

Refresh of the HM4716A is accomplished by performing A memory cycle at each of the 128 row addresses within each two millisecond time interval.
Any cycle in which $\overline{RE}$ signal occurs refreshes the entire selected row.
$\overline{RE}$-only refresh results in substantial reduction in operating power.
This reduction in power is reflected in the IDD3 specification.

• PAGE MODE;

Page mode operation allows faster successive memory operations at multiple column locations of the same row address with increased speed.
This is done by strobing the row address into the chip and maintaining $\overline{RE}$ at a logic low throughout all successive $\overline{CE}$ memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be decreased and the operating power is reduced. These are reflected in the TCELQV, TCEHCEL, IDD4 specifications.

HM4816

16384-word×1-bit Dynamic Random Access Memory

The HM4816 is a new generation MOS dynamic RAM circuit organized as 16,384 words by 1 bit. As a state-of-the art MOS memory device, the HM4816 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK4027 (4K RAM).

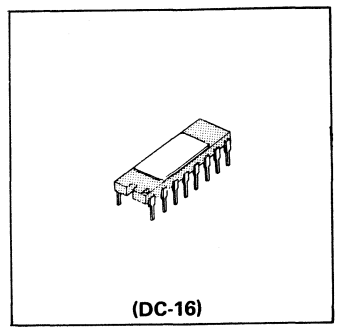
The technology used to fabricate the HM4816 is HITACHI's double-poly, N-channel silicon gate process.

This process, coupled with the use of a single transistor dynamic storage cell provides the maximum possible circuit density and reliability, while maintaining high performance capability.

The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the HM4816 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMs) permits the HM4816 to be packaged in a standard 16-pin DIP.

This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

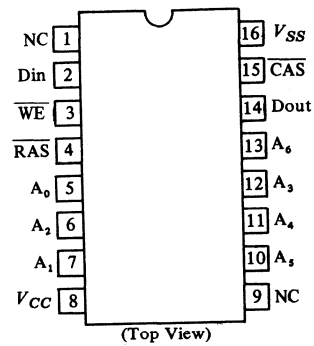


(DC-16)

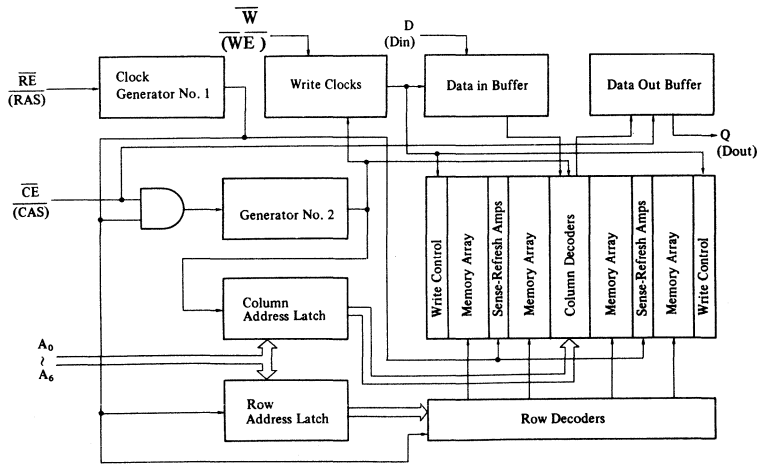
■ FEATURES

- Single 5V supply
- Low power standby and operation
  (Standby: 55mW max, operation: 440mW max)
- Fast access time & cycle time
  (access time: 100ns max, cycle time: 200ns min)
- Directly TTL compatible: All inputs & outputs
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read modify write, $\overline{RAS}$ only refresh and page mode capability

■ PIN ARRANGEMENT



(Top View)



HITACHI

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM4816	Unit
Voltage on any pin relative to GND	V_T	−1.0~+7.0	V
Power supply voltage relative to GND	V_{CC}	−0.5~+7.0	V
Short-circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0~+70	°C
Storage Temperature	T_{stg}	−65~+150	°C

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Units	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1,2
Input high(logic 1) voltage $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IHC}	2.7	—	6.0	V	1
Input high(logic 1) voltage except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IH}	2.7	—	6.0	V	1
Input low(logic 0) voltage all inputs	V_{IL}	−1.0	—	0.8	V	1

Notes: 1. All voltages referenced to V_{SS}.
2. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading.

■ DC ELECTRICAL CHARACTERISTICS

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC}=200ns, Note 2	—	—	80	mA
Standby current	I_{CC2}	$\overline{RAS}=V_{IHC}$, Dout=high impedance	—	—	10	mA
Refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}=V_{IHC}$; t_{RC}=200ns	—	—	55	mA
Page mode current	I_{CC4}	$\overline{RAS}=V_{IL}$, $\overline{CAS}$ cycling, t_{PC}=120ns; Note 2	—	—	55	mA
Input leakage current	$I_{I(L)}$	V_{IN}=0 to 6V, all other pins=0V	−10	—	10	μA
Output leakage current	$I_{O(L)}$	V_{OUT}=0 to 5.5V, Dout is disabled	−10	—	10	μA
Output high voltage	V_{OH}	Note 1, I_{out}=−5mA	2.4	—	V_{CC}	V
Output low voltage	V_{OL}	I_{OUT}=4.2mA	—	—	0.4	V

Notes: 1. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading.

2. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

■ A.C. ELECTRICAL CHARACTERISTICS (Ta=0 to 70℃, V_{CC}=5.0V±10%)

Item	Symbol	min.	typ.	max.	Unit	Note
Random read or write cycle Time	t_{RC}	200	—	—	ns	3
Read-write Cycle Time	t_{RWC}	200	—	—	ns	3
Page Mode Cycle Time	t_{PC}	120	—	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	—	100	ns	4, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	—	65	ns	5, 6
Output Buffer Turn-off Delay	t_{OFF}	0	—	25	ns	7
Transition Time (rise & fall)	t_T	3	—	25	ns	2
$\overline{RAS}$ Precharge	t_{RP}	65	—	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	—	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	65	—	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	65	—	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	15	—	35	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	40	—	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	—	ns	
Row Address Hold Time	t_{RAH}	15	—	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	—	ns	
Column Address Hold Time	t_{CAH}	35	—	—	ns	
Column Address Hold Time reference to $\overline{RAS}$	t_{AR}	70	—	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	—	ns	
Read Command Hold Time	t_{RCH}	10	—	—	ns	
Write Command Hold Time	t_{WCH}	40	—	—	ns	
Write Command Hold Time reference to $\overline{RAS}$	t_{WCR}	75	—	—	ns	
Write Command Pulse Width	t_{WP}	30	—	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	45	—	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	45	—	—	ns	
Data-in Set-up Time	t_{DS}	0	—	—	ns	9
Data-in Hold Time	t_{DH}	40	—	—	ns	9
Data-in Hold Time reference to $\overline{RAS}$	t_{DHR}	75	—	—	ns	
$\overline{CAS}$ Precharge Time (for page mode cycle only)	t_{CPP}	40	—	—	ns	
Refresh Period	t_{REF}	—	—	2	ns	
$\overline{WE}$ Command Set-up Time	t_{WCS}	−10	—	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	45	—	—	ns	10
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	80	—	—	ns	10
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	—	ns	

NOTES:

1. AC measurements assume t_T = 5ns.
2. V_{IHC}(min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
3. The specification for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C + T_a \leqq 70°C$) is assured.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

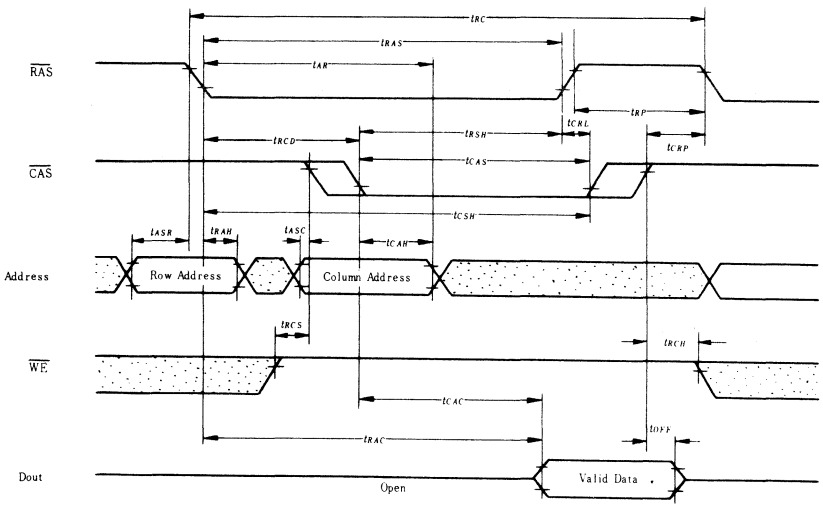
■ CAPACITANCE (Ta=0 to 70℃, V_{CC}=5.0V±10%)

Item	Symbol	min.	typ.	max.	Unit	Note
Input Capacitance (A_0 to A_6), Din	C_{I1}	—	4	6	pF	1
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}	—	5	7	pF	2
Output Capacitance (Dout)	C_O	—	5	7	pF	2, 3

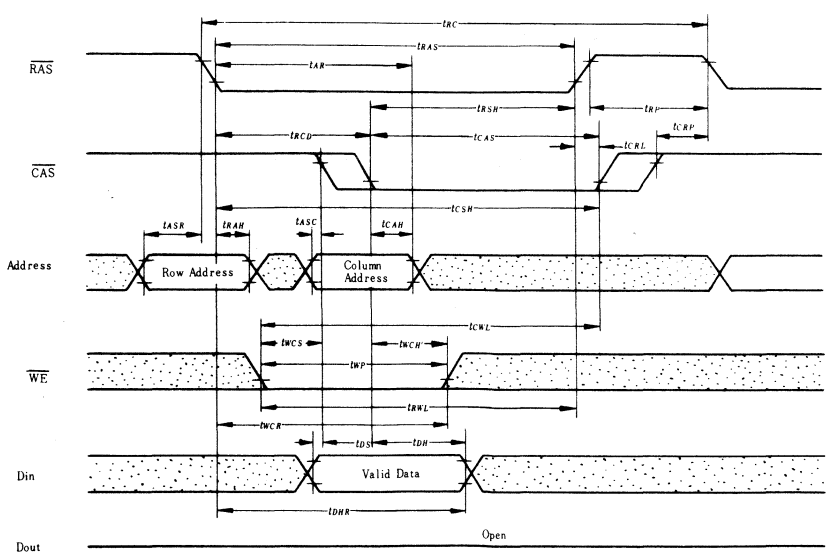
Notes: 1. Effective capacitance calculated from the equation $C = I \cdot \Delta t/\Delta V$ with ΔV = 3V and power supplies at nominal levels.

2. $\overline{CAS}$ = V_{IHC} to disable D_{OUT}.

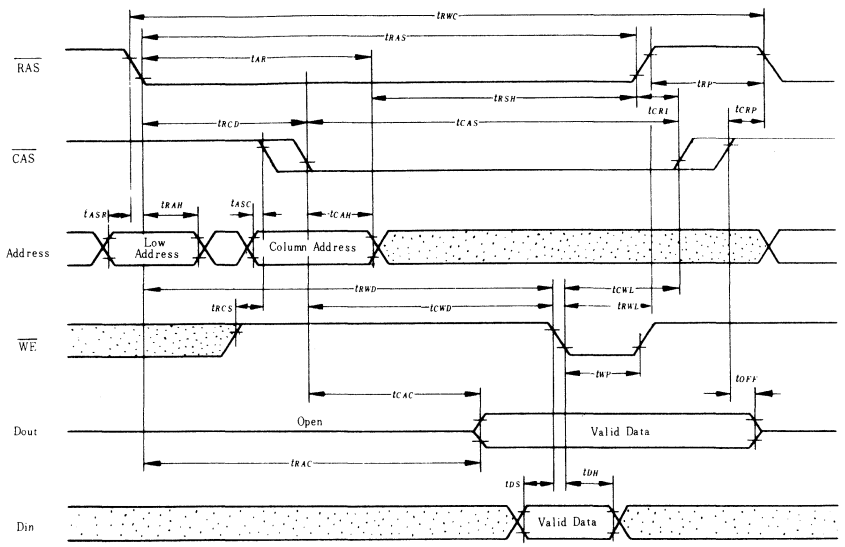
• READ CYCLE



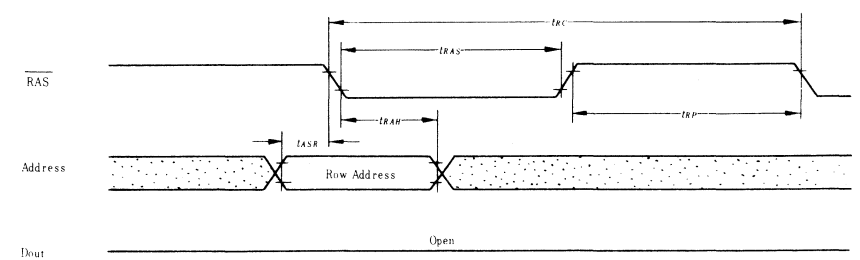
• WRITE CYCLE



• READ-WRITE/READ-MODIFY-WRITE CYCLE

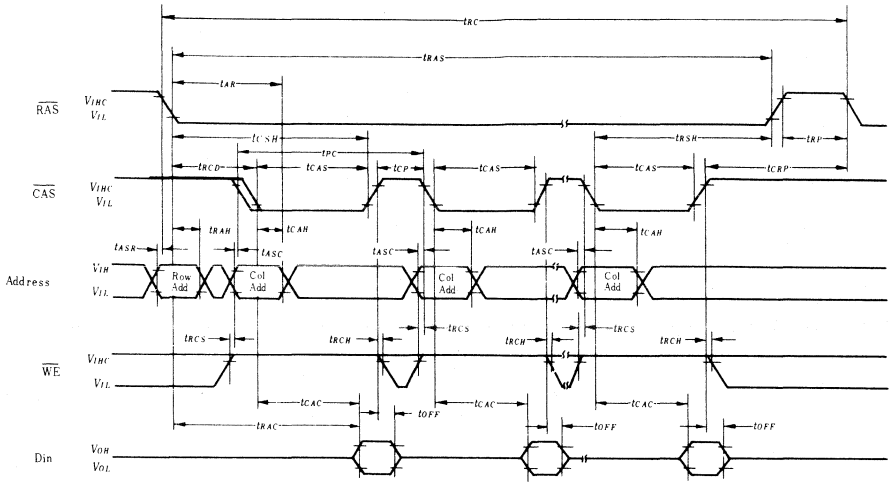


• RAS-ONLY" REFRESH CYCLE

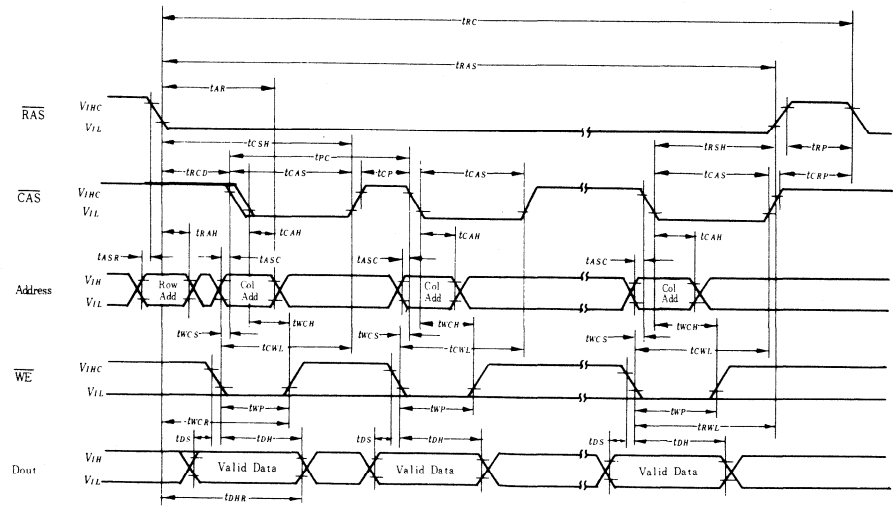


Note: $\overline{CAS} = V_{IHC}$

• PAGE MODE READ CYCLE



• PAGE MODE WRITE CYCLE



HM4864-2, HM4864-3 — Preliminary

65536-word X 1-bit Dynamic Random Access Memory

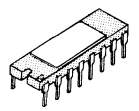
The HM4864 is a 65,536-words by 1-bit, MOS random access memory circuit fabricated with HITACHI's double-poly N-channel silicon gate process for high performance and high functional density. The HM4864 uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.

Multiplexed address inputs permit the HM4864 to be packaged in a standard 16 pin DIP on 0.3 inch centers.

This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of +5V with ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The HM4864 also incorporates several flexible timing/operating modes.

In addition to the usual read, write, and read-modify-write cycles, the HM4864 is capable of delayed write cycles, page-mode operation and $\overline{RAS}$-only refresh.

Proper control of the clock inputs ($\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

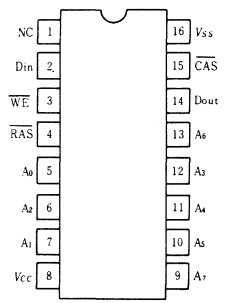


(DC-16)

■ FEATURES

- Recognized industry standard 16-pin configuration
- 150ns access time, 270ns cycle (HM4864-2)
  200ns access time, 335ns cycle (HM4864-3)
- Single power supply of +5V±10% with a built-in V_{BB} generator
- Low Power; 330 mW active. 20 mW standby (max)
- The inputs TTL compatible, low capacitance, and protected against static charge
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability
- 128 refresh cycle

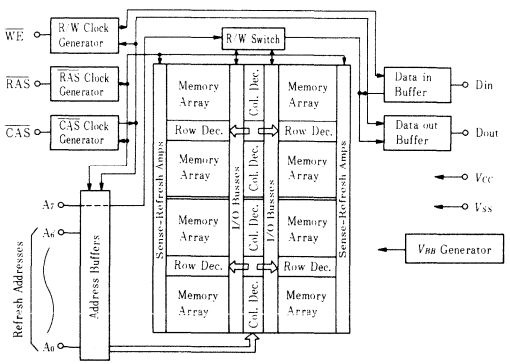
■ PIN ARRANGEMENT



(Top View)

A_0-A_7	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_0-A_6	Refresh Address Strobe

■ FUNCTIONAL DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . −1.0 to +7V
Operating Temperature, Ta (Ambient) . . . . . 0 to +70°C
Storage Temperature (Ambient) . . . . . −65 to +150°C
Short-circuit Output Current . . . . . 50 mA
Power Dissipation . . . . . 1 W

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	–	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	–	0.8	V	1

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V±10%, V_{SS} = 0V)

Parameter	Symbol	min.	max.	Unit	Notes
OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC}=min.)	I_{CC1}	–	60	mA	2, 4
STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = V_{IH}, D_{out} = High Impedance)	I_{CC2}	–	3.5	mA	
REFRESH CURRENT Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}	–	4.5	mA	
PAGE MODE CURRENT Average Power Supply Current, Page-mode Operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling; t_{PC} = min.)	I_{CC4}	–	45	mA	4
INPUT LEAKAGE Input Leakage Current, any Input (V_{in} = 0 to +6.5V, all other pins not under test = 0V)	I_{IL}	−10	10	μA	
OUTPUT LEAKAGE Output Leakage Current (D_{out} is disabled, V_{out} = 0 to +5.5V)	I_{OL}	−10	10	μA	3
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{out} = −5mA)	V_{OH}	2.4	V_{CC}	V	
Output Low (Logic 0) Voltage (I_{out} = 4.2mA)	V_{OL}	0	0.4	V	

NOTES
1. All voltages referenced to V_{SS}.
2. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
3. I_{OL} consists of leakage current only.
4. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

■ AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	typ.	max.	Unit	Notes
Input Capacitance (A_0-A_7, D_{in})	C_{in1}	–	7	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{in2}	–	10	pF	1
Output Capacitance (D_{out})	C_{out}	–	7	pF	1, 2

NOTES
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS[1), 2)]

(T_a = 0 to +70°C, V_{CC} = 5V±10%, V_{SS} = 0V)

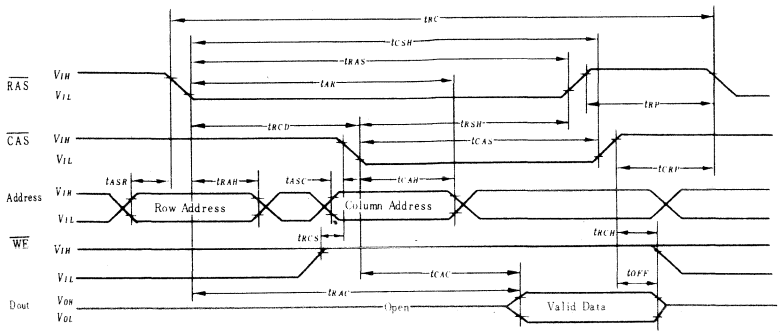
Parameter	Symbol	HM4864-2		HM4864-3		Unit	Notes
		min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	270	–	335	–	ns	
Read-Write Cycle Time	t_{RWC}	270	–	335	–	ns	
Page Mode Cycle Time	t_{PC}	170	–	225	–	ns	
Access Time from $\overline{RAS}$	t_{RAC}	–	150	–	200	ns	4, 6
Access Time from $\overline{CAS}$	t_{CAC}	–	100	–	135	ns	5, 6
Output Buffer Turn-off Delay	t_{OFF}	0	40	0	50	ns	7
Transition Time (Rise and Fall)	t_T	3	35	3	50	ns	3
$\overline{RAS}$ Precharge Time	t_{RP}	100	–	120	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	150	10000	200	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100	–	135	–	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	100	–	135	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	150	–	200	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	25	65	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−20	–	−20	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	20	–	25	–	ns	
Column Address Set-up Time	t_{ASC}	−10	–	−10	–	ns	
Column Address Hold Time	t_{CAH}	45	–	55	–	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	95	–	120	–	ns	
Read Command Set-up Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	ns	
Write Command Hold Time	t_{WCH}	45	–	55	–	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	95	–	120	–	ns	
Write Command Pulse Width	t_{WP}	45	–	55	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	45	–	55	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	45	–	55	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	45	–	55	–	ns	9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	95	–	120	–	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	60	–	80	–	ns	
Refresh Period	t_{REF}	–	2	–	2	ms	
$\overline{WE}$ Command Set-up Time	t_{WCS}	−20	–	−20	–	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Delay	t_{CWD}	60	–	80	–	ns	10
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	110	–	145	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	–	0	–	ns	

NOTES

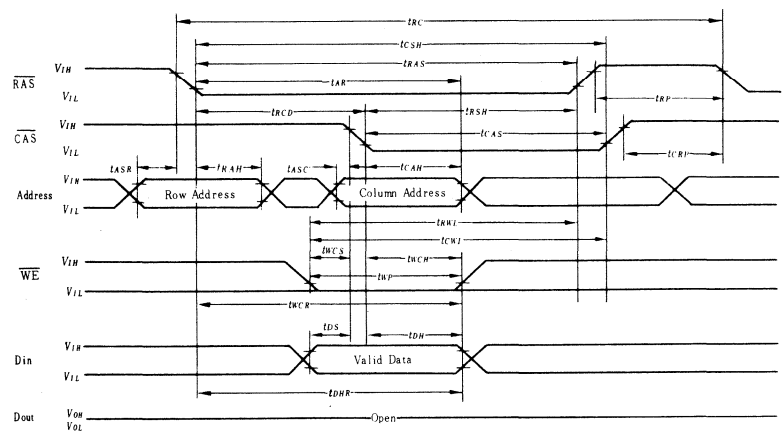
1. AC measurements assume t_T = 5ns.
2. 8 cycles are required after power-on or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} = t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
5. Assumes that $t_{RCD} = t_{RCD}$ (max).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} = t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} = t_{CWD}$ (min) and $t_{RWD} = t_{RWD}$ (min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

■ TIMING WAVEFORMS

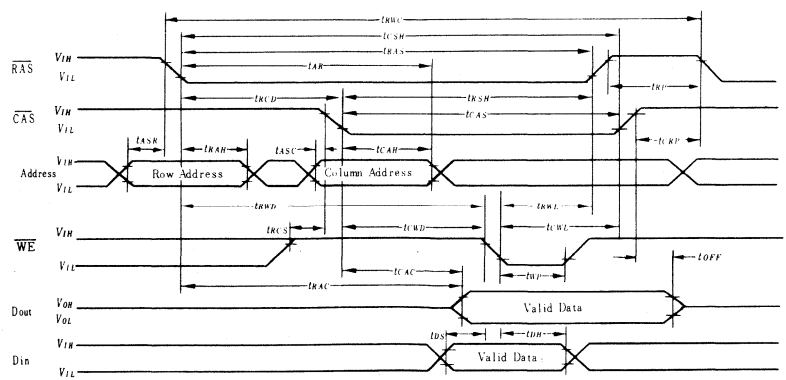
• READ CYCLE



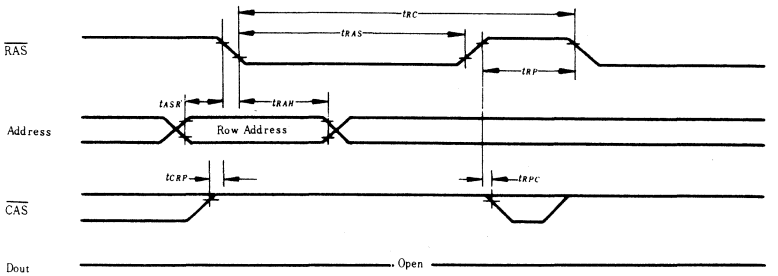
• WRITE CYCLE



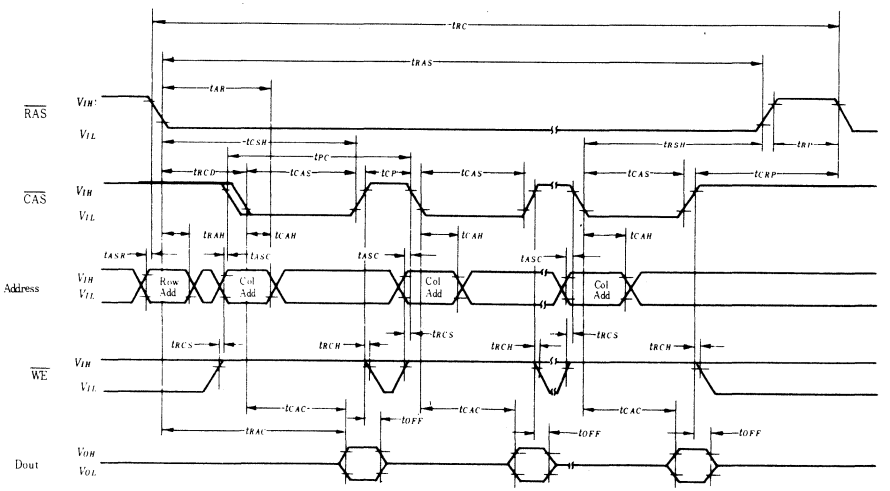
• READ-WRITE/READ-MODIFY-WRITE CYCLE



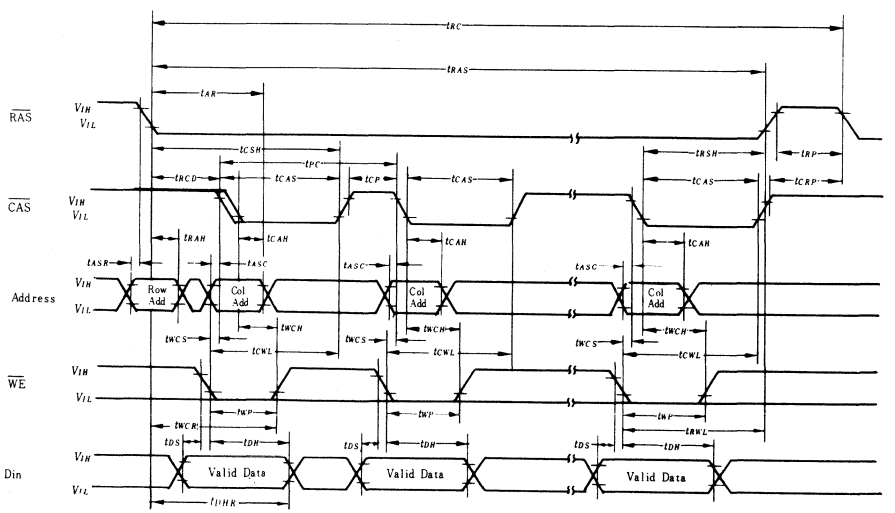
- **"$\overline{\text{RAS}}$-ONLY" REFRESH CYCLE**



- **PAGE MODE READ CYCLE**

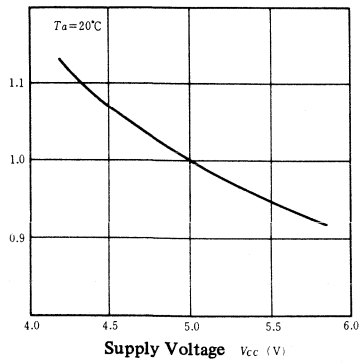


- **PAGE MODE WRITE CYCLE**

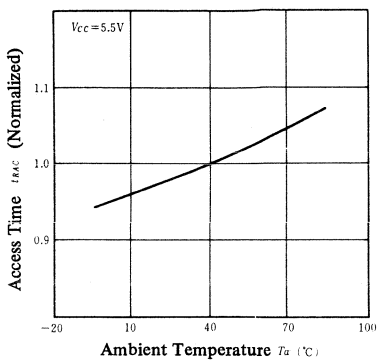


TYPICAL CHARACTERISTICS

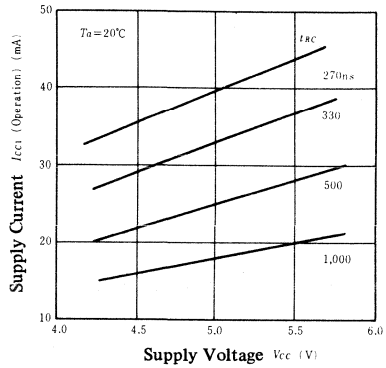
ACCESS TIME vs. SUPPLY VOLTAGE



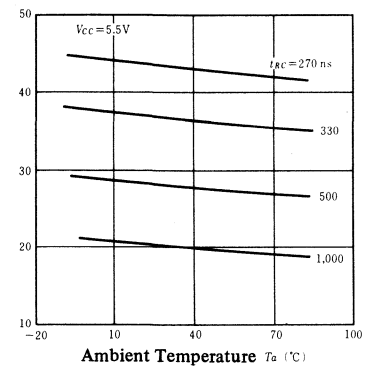
ACCESS TIME vs. AMBIENT TEMPERATURE



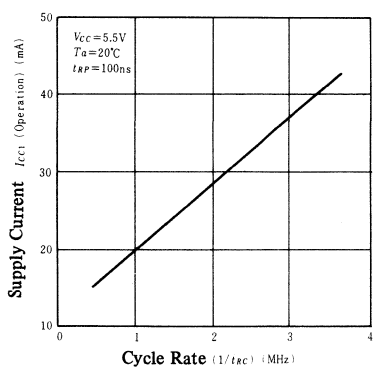
SUPPLY CURRENT vs. SUPPLY VOLTAGE



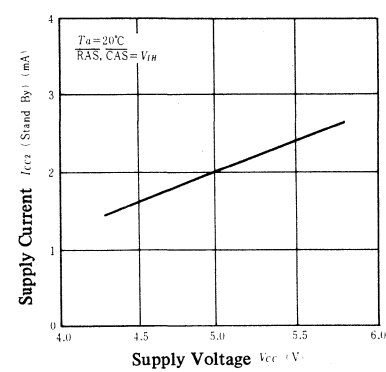
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



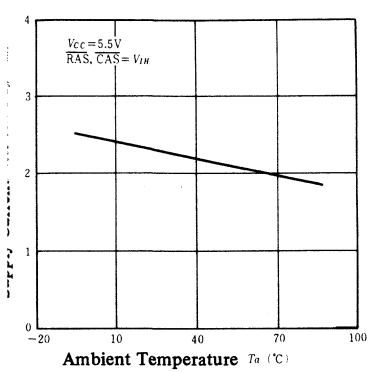
SUPPLY CURRENT vs. CYCLE RATE



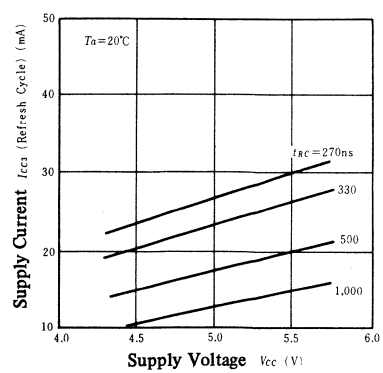
SUPPLY CURRENT vs. SUPPLY VOLTAGE



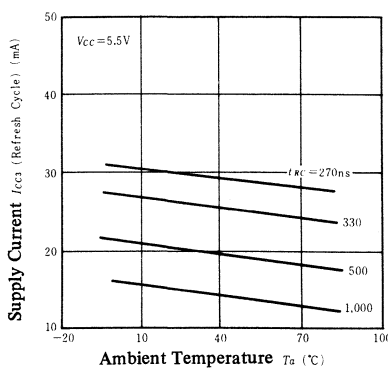
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



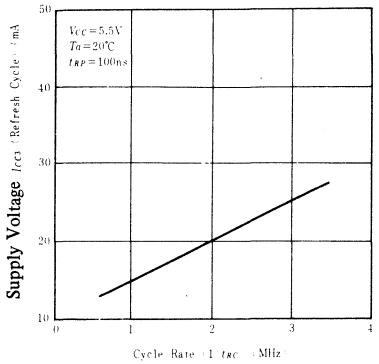
SUPPLY CURRENT vs. SUPPLY VOLTAGE



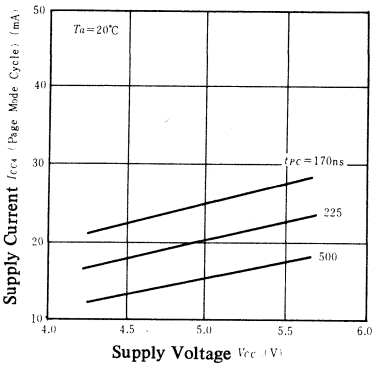
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



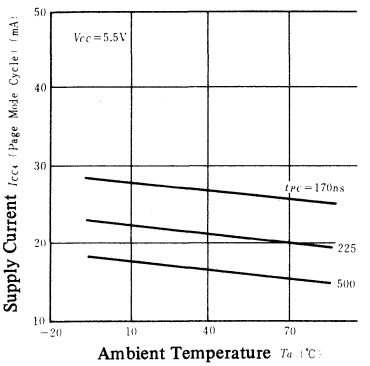
SUPPLY CURRENT vs. CYCLE RATE



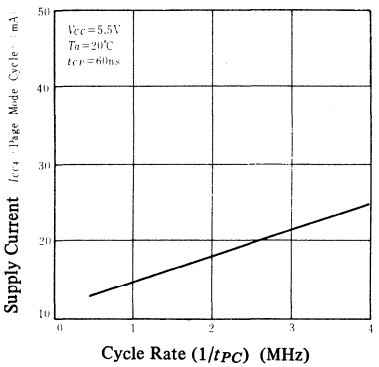
SUPPLY CURRENT vs. SUPPLY VOLTAGE



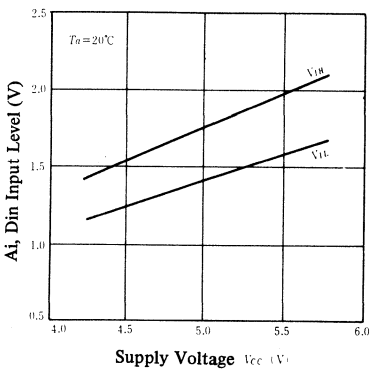
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



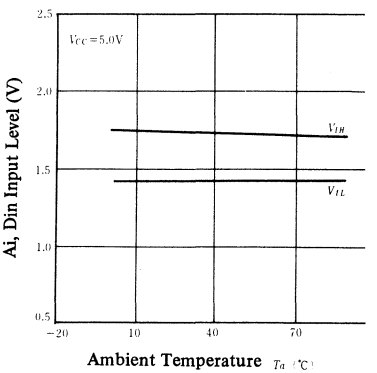
SUPPLY CURRENT vs. CYCLE RATE



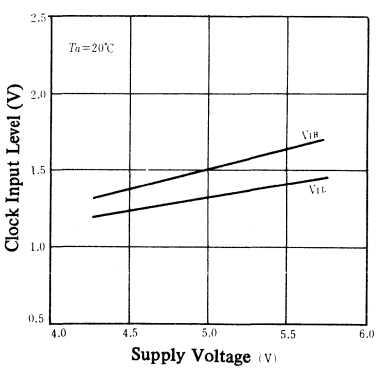
INPUT LEVEL vs. SUPPLY VOLTAGE



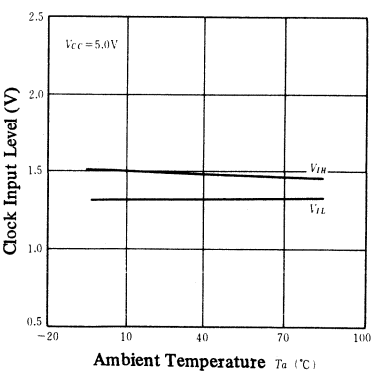
INPUT LEVEL vs. AMBIENT TEMPERATURE

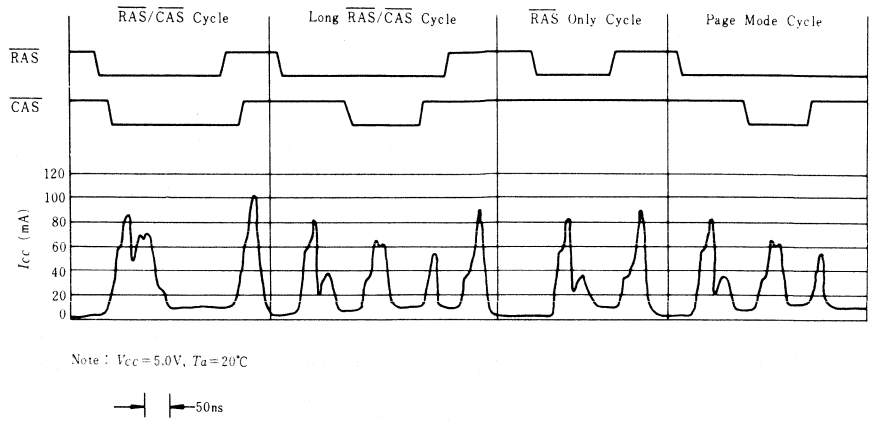


CLOCK INPUT LEVEL vs. SUPPLY VOLTAGE



CLOCK INPUT LEVEL vs. AMBIENT TEMPERATURE





■ APPLICATION INFORMATION

• POWER ON

An initial pause of 500 μs is required after power-up followed by a minimum of eight (8) initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh) prior to normal operation.

The V_{CC} current (I_{CC}) requirement of the HM4864 during power on is, however, dependent upon the input levels ($\overline{RAS}$, $\overline{CAS}$) and the rise time of V_{CC}, as shown in Fig. 1.

• READ CYCLE

A read cycle begins with addresses stable and a negative going transition of $\overline{RAS}$. The time delay between the stable address and the start of $\overline{RAS}$-on is controlled by parameter t_{ASR}.

Following the time when $\overline{RAS}$ reaches its low level, the row address must be held stable long enough to be captured. This controlling parameter is t_{RAH}. Following this interval, the address can be changed from row address to column address. When the column address is stable, $\overline{CAS}$ can be turned on. The leading edge of $\overline{CAS}$ is controlled by parameter t_{RCD}. The basic limit on the $\overline{CAS}$ leading edge is that $\overline{CAS}$ can not start untill the column address is stable, and this is controlled by parameter t_{ASC}. The column address must be held stable long enough to be captured. The controlling parameter is t_{CAH}. Note that t_{RCD} (max) is not an operating limit of the HM4864 though its specification is listed on the data sheets. If $\overline{CAS}$ becomes on later than t_{RCD} (max), the access time from $\overline{RAS}$ will be increase by the time which t_{RCD} exceeds t_{RCD} (max). Following the time when $\overline{CAS}$ reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is t_{CAC}-access time from $\overline{CAS}$.

The access time from $\overline{RAS}$-t_{RAC}-is the time from $\overline{RAS}$-on to valid Dout.

The minimum value of t_{RAC} is derived as the sum of t_{RCD} (max) and t_{CAC}.

The selected output data is held valid internally until $\overline{CAS}$ becomes high, and then Dout pin becomes high impedance. This parameter is t_{OFF}.

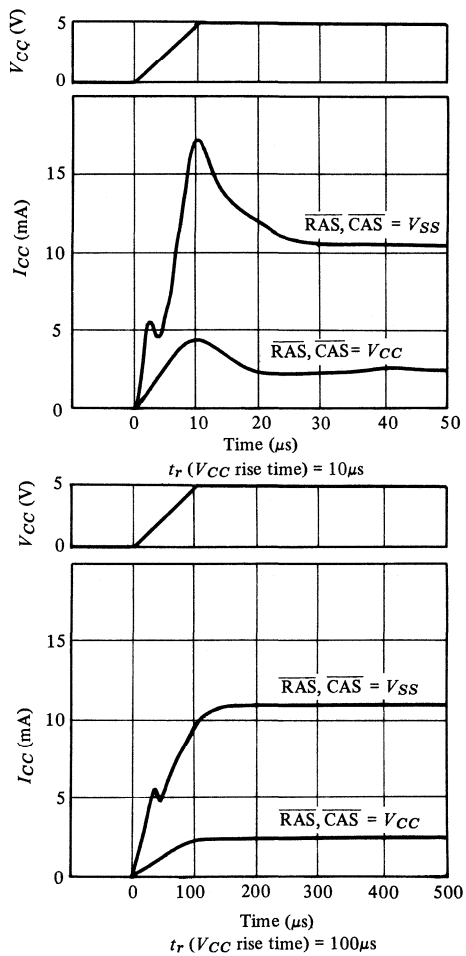


Fig. 1 Typical I_{CC} vs. V_{CC} during power up.

- **WRITE CYCLE**

A write cycle is performed by bringing $\overline{WE}$ low before or during $\overline{CAS}$-on.
Two different write cycles can be defined as;
Write cycle-Write data are available at the beginning of the $\overline{CAS}$-on so that the write operation starts at the beginning. In this mode, Dout and $\overline{WE}$ signal times are not in any critical path for determining cycle time.
Following the time when $\overline{WE}$ reaches its low level, $\overline{WE}$ must be held stable long enough to be captured. This $\overline{WE}$-on pulse deration is called t_{WP}. The time required to capture write data in a latch is called t_{DH}. This cycle is called an "early write".

Read Write cycle- This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated.
$\overline{WE}$ and Din are delayed until after Dout. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, Din and $\overline{WE}$ become critical path signals for determining cycle time.

- **CLOCK-OFF TIMING**

$\overline{RAS}$ and $\overline{CAS}$ must stay on for Dout stabilized to valid data. In the case of $\overline{CAS}$, this is controlled by parameter t_{CAS} (min). In the case of $\overline{RAS}$, this is controlled by parameter t_{RSH} (min). Following the end of $\overline{RAS}$, $\overline{CAS}$ must stay off long enough to precharge internal circuits. The only parameter of concern is t_{RP}. Normally $\overline{CAS}$ is not required to be off for minimum time of t_{CRP}. However, in a page mode memory operation, there is a t_{CP} (min) specification to control the $\overline{CAS}$-off time.

- **DATA OUTPUT**

Dout is three-state TTL compatible with a fan-out of two standard TTL loads.
When $\overline{CAS}$ is high, Dout is in a high impedance state. When $\overline{CAS}$ is low, valid data appears after t_{CAC} at a read cycle, and Dout is not valid at an early-write cycle.

- **REFRESH**

Refresh of the HM4864 is accomplished by performing memory cycle at each of the 128 row addresses within eac two millisecond time interval.
A0 to A6 are refresh address pin compatible with standar 16K RAM (HM4716A, HM4816). Any cycle in which $\overline{RA}$ signal occurs refreshes the entire selected row. $\overline{RAS}$-onl refresh results in substantial reduction in operating powe This reduction in power is reflected in the I_{CC3} specification.

- **PAGE MODE**

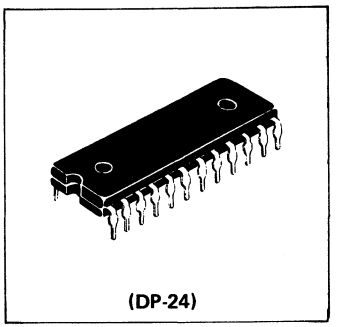
Page mode operation allows faster successive memory oper tions at multiple colum locations of the same row address wit increased speed.
This is done by strobing the row address into the chip an maintaining $\overline{RAS}$ at a logic low throughout all successive $\overline{CA}$ memory cycles in which the row address is latched. As th time normally required for strobing a new row address eliminated, access and cycle times can be decreased and th operating power is reduced. These are specifications.

MOS ROM

HN462316EP

2048-word×8-bit Mask-Programmable Read Only Memory

The HN462316EP is a mask-programmable, byte-organized memory designed for use in bus-organized systems.
To facilitate use, the device operates from a single power supply, has compatibility with TTL and DTL, and requires no clocks or refreshing because of static operation.
Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are to be defined by the customer.

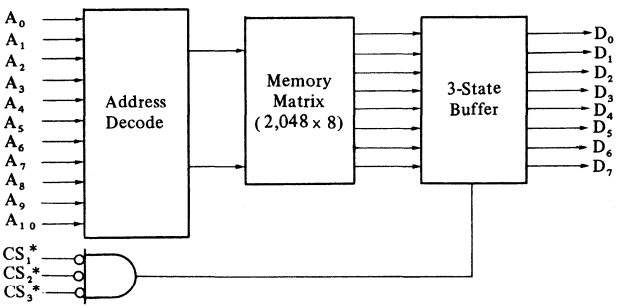


(DP-24)

■ FEATURES

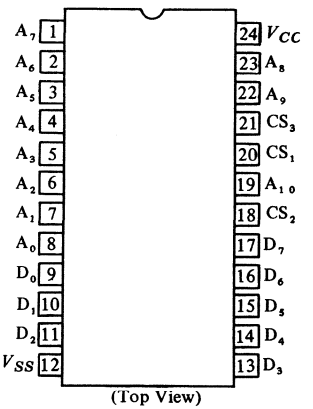
- Three-state Data Output
- Three Chip Select Inputs (Programmable)
- Single 5V Power Supply
- TTL Compatible
- Maximum Access Time; 350ns
- N-channel Si Gate MOS Technology
- EPROM/ROM Pin Compatible for Cost-Effective System Development

■ BLOCK DIAGRAM



*Active level defined by the customer.

■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

*With respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Input Voltage	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.0	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	°C

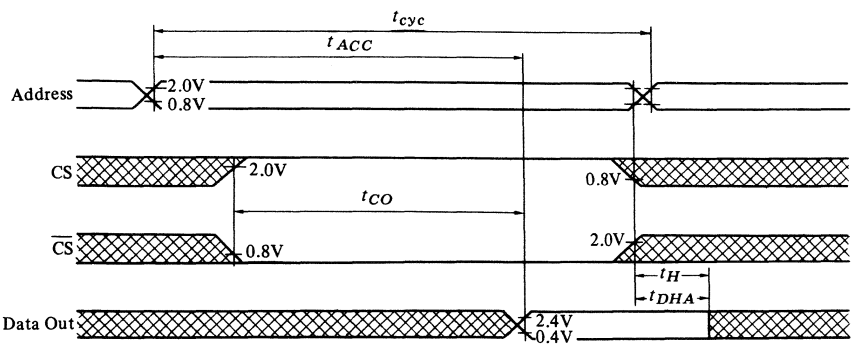
■ ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V±10%, V_{SS}=0V, Ta=−20 to +75℃ unless otherwise noted)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input High-level Voltage	V_{IH}	—	2.0	—	V_{CC}	V
Input Low-level Voltage	V_{IL}	—	−0.3	—	0.8	V
Output High-level Voltage	V_{OH}	I_{OH}=−100μA	2.4	—	—	V
Output Low-level Voltage	V_{OL}	I_{OL}=1.6mA	—	—	0.4	V
Input Leakage Current	I_{in}	V_{in}=0 to 5.5V	—	—	2.5	μA
Output High-level Leakage Current	I_{LOH}	V_{out}=2.4V, CS=0.8V, $\overline{CS}$=2.0V	—	—	10	μA
Output Low-level Leakage Current	I_{LOL}	V_{out}=0.4V, CS=0.8V, $\overline{CS}$=2.0V	—	—	10	μA
Supply Current	I_{CC}	V_{CC}=5.5V	—	—	120	mA
Input Capacitance	C_{in}	V_{in}=0V, f=1.0MHz, Ta=25℃	—	—	7.5	pF
Output Capacitance	C_{out}	V_{in}=0V, f=1.0MHz, Ta=25℃	—	—	12.5	pF

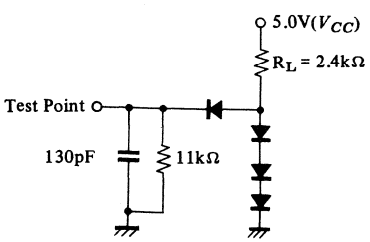
■ AC OPERATING CONDITIONS AND CHARACTERISTICS

• READ SEQUENCE

Item	Symbol	min.	max.	Unit
Cycle Time	t_{CYC}	350	—	ns
Access Time	t_{ACC}	—	350	ns
Chip Select to Output Delay	t_{CO}	—	150	ns
Data Hold Time from Address	t_{DHA}	10	—	ns
Data Hold Time from Deselection	t_H	10	150	ns



• LOAD CIRCUIT



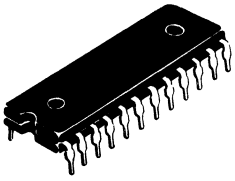
Notes: 1. $t_r = t_f$ = 20 ns
2. C_L includes jig capacitance
3. All diodes are 1S2074Ⓗ

HN46332P

4096-word X 8-bit Mask Programmable Read Only Memory

The HN46332P is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL and DTL, and requires no clocks or refreshing because of static operation.

The memory is compatible with the HMCS6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

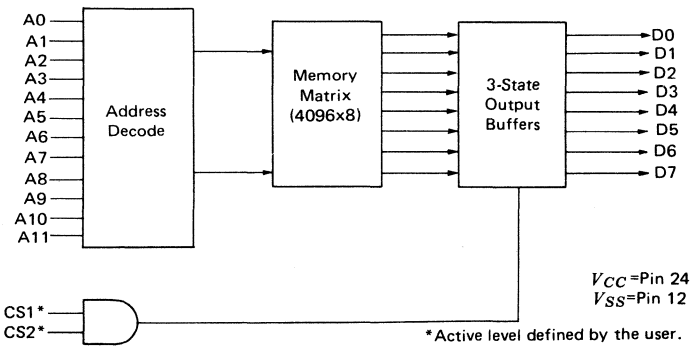


(DP-24)

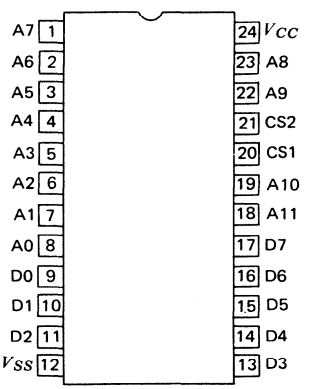
■ FEATURES

- Fully Static operation
- Three-State Data Output for OR-Ties
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single +5-Volt Power Supply
- Fully TTL Compatible
- Maximum Access Time=350ns
- N-Channel Si Gate MOS Technology
- Pin Compatible with EPROMs

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

*With respect to V_{SS}.

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.3	–	0.8	V
	V_{IH}	2.0	–	V_{CC}	V
Operating Temperature	T_{opr}	−20	–	75	°C

■ ELECTRICAL CHARACTERISTICS

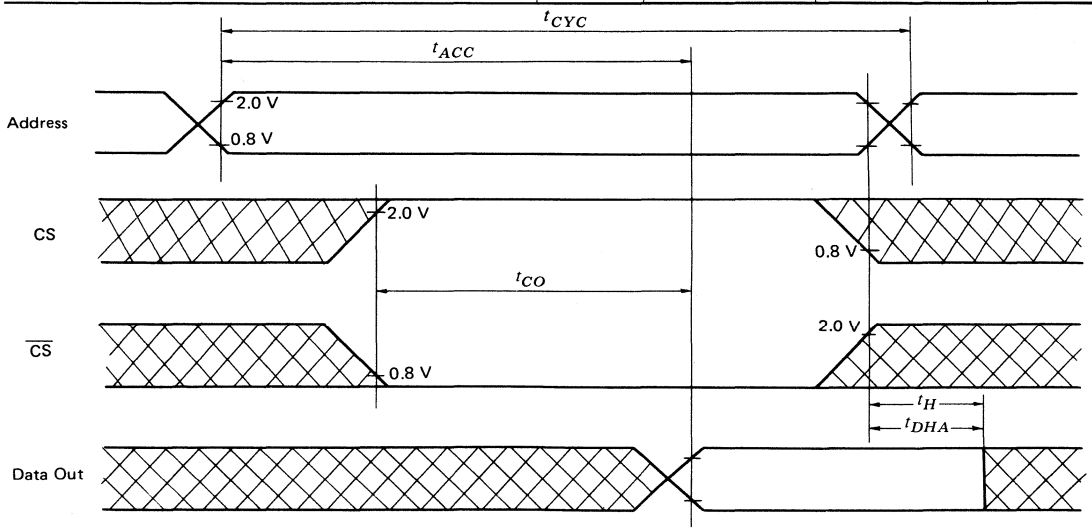
(V_{CC} = 5.0V ±10%, V_{SS} = 0V, T_a = −20 to +75°C unless otherwise noted)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input High-level Voltage	V_{IH}	—	2.0	—	V_{CC}	V
Input Low-level Voltage	V_{IL}	—	−0.3	—	0.8	V
Output High-level Voltage	V_{OH}	I_{OH} = −100μA	2.4	—	—	V
Output Low-level Voltage	V_{OL}	I_{OL} = 1.6mA	—	—	0.4	V
Input Leakage Current	I_{in}	V_{in} = 0 to 5.5V	—	—	2.5	μA
Output High-level Leakage Current	I_{LOH}	V_{out} = 2.4V, CS = 0.8V, $\overline{CS}$ = 2.0V	—	—	10	μA
Output Low-level Leakage Current	I_{LOL}	V_{out} = 0.4V, CS = 0.8V, $\overline{CS}$ = 2.0V	—	—	10	μA
Supply Current	I_{CC}	V_{CC} = 5.5V	—	—	80	mA
Input Capacitance	C_{in}	V_{in} = 0V, f = 1.0MHz, T_a = 25°C	—	—	7.5	pF
Output Capacitance	C_{out}	V_{in} = 0V, f = 1.0MHz, T_a = 25°C	—	—	12.5	pF

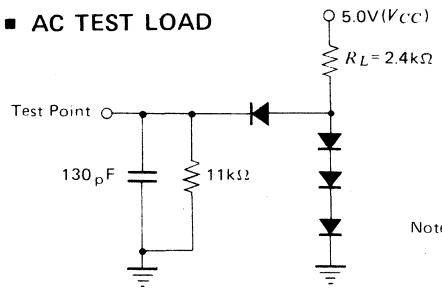
■ AC OPERATING CONDITIONS AND CHARACTERISTICS

• READ SEQUENCE

Item	Symbol	min.	max.	Unit
Cycle Time	t_{CYC}	350	—	ns
Access Time	t_{ACC}	—	350	ns
Chip Select to Output Delay	t_{CO}	—	150	ns
Data Hold Time from Address	t_{DHA}	10	—	ns
Data Hold Time from Deselection	t_H	10	150	ns



■ AC TEST LOAD



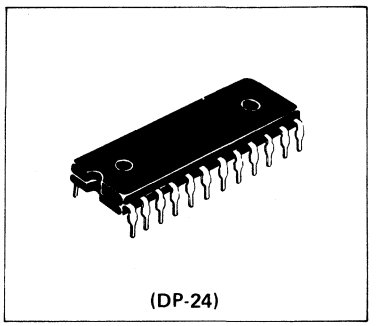
Notes: 1. $t_r = t_f$ = 20ns
2. C_L includes jig capacitance
3. All diodes are 1S2074 (H)

HN48364P

8192-word X 8-bit Mask Programmable Read Only Memory

The HN48364P is a mask-programmable, byte-oraganized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL and DTL, and requires no clocks or refreshing because of static operation.

The memory is compatible with the HMCS6800 Microcomputer Family, providing read only storage in byte increments. The active level of the Chip Enable input and the memory content are defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

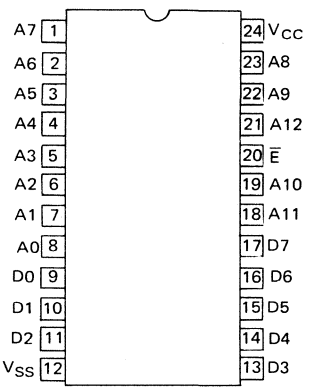


(DP-24)

■ FEATURES

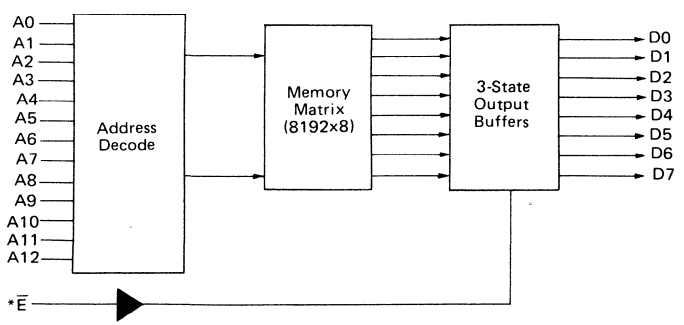
- Fully Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Enable
- TTL Compatible
- Maximum Access Time-350ns
- Pin Compatible with EPROMs

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



*Active level defined by the user.

V_{CC}=Pin 24
V_{SS}=Pin 12

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

*With respect to V_{SS}.

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.3	–	0.8	V
	V_{IH}	2.0	–	V_{CC}	V
Operating Temperature	T_{opr}	−20	–	75	°C

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, V_{SS} = 0V, T_a = −20 to +75°C unless otherwise noted.)

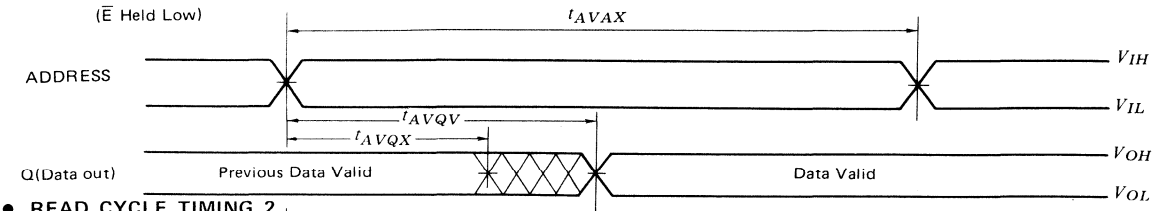
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input High-level Voltage	V_{IH}	–	2.0	–	V_{CC}	V
Input Low-level Voltage	V_{IL}	–	−0.3	–	0.8	V
Output High-level Voltage	V_{OH}	I_{OH} = −205μA	2.4	–	–	V
Output Low-level Voltage	V_{OL}	I_{OL} = 3.2mA	–	–	0.4	V
Input Leakage Current	I_{in}	V_{in} = 0 to 5.5V	–	–	2.5	μA
Output High-level Leakage Current	I_{LOH}	V_{out} = 2.4V, E = 0.8V, $\overline{E}$ = 2.0V	–	–	10	μA
Output Low-level Leakage Current	I_{LOL}	V_{out} = 0.4V, E = 0.8V, $\overline{E}$ = 2.0V	–	–	10	μA
Supply Current (Active/Standby)	$I_{CC/Isb}$	V_{CC} = 5.5V	–	45/6	80/10	mA
Input Capacitance	C_{in}	V_{in} = 0V, f = 1.0MHz, T_a = 25°C	–	–	7.5	pF
Output Capacitance	C_{out}	V_{in} = 0V, f = 1.0MHz, T_a = 25°C	–	–	12.5	pF

■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

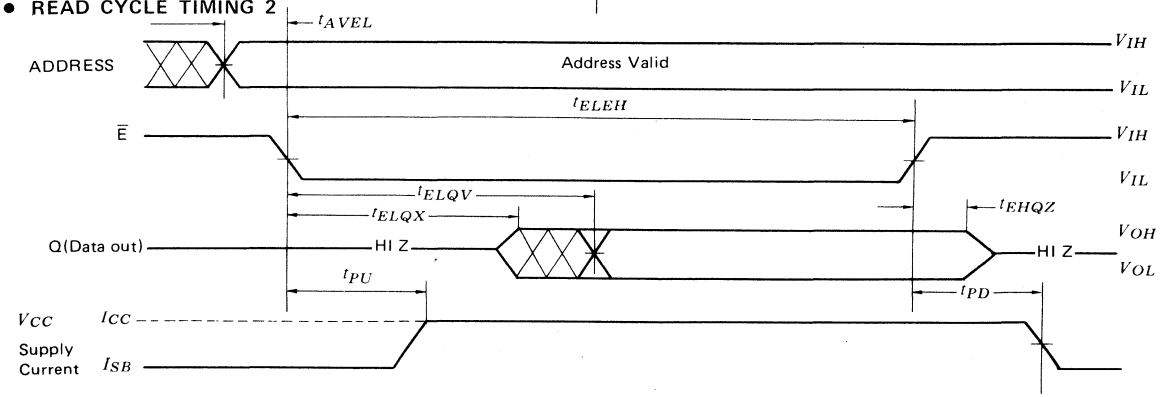
(V_{CC} = 5.0V ±10%, T_a = −20 to +75°C, All timing with t_r = t_f = 20ns)

Item	Symbol	min.	max.	Unit
Address Valid to Address Don't Care (Cycle Time when Chip Enable is held Active)	t_{AVAX}	350	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	350	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	–	350	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	–	350	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	ns
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	ns
Chip Enable High to Output High Z	t_{EHQZ}	0	80	ns
Chip Selection to Power Up Time	t_{PU}	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	120	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	ns

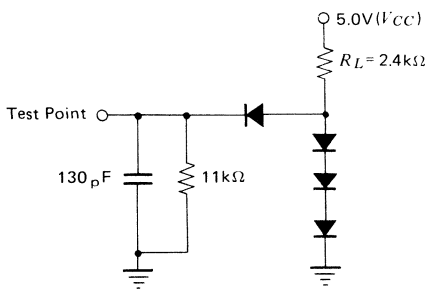
• READ CYCLE TIMING 1



• READ CYCLE TIMING 2



■ AC TEST LOAD



Notes: 1. t_r=t_f=20ns
2. C_L includes jig capacitance
3. All diodes are 1S2074 (H)

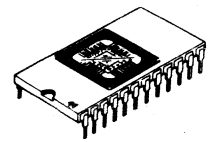
HN462716, HN462716G

2048-word×8-bit UV Erasable and Electrically Programmable Only Memory

The HN462716 is a 2048 word by 8 bit erasable and electrically programmable ROMs. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

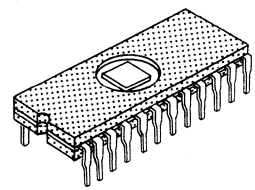
- Single Power Supply ..... +5V ±5%
- Simple Programming .....Program Voltage: +25V DC
  Programs with One 50ms Pulse
- Static ..... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded-on Chip Address Decode
- Access Time ..... 450ns Max.
- Low Power Dissipation .....555mW Max. Active Power
  213mW Max. Standby Power
- Three State Output ..... OR-Tie Capability
- Interchangeable with Intel 2716

HN462716



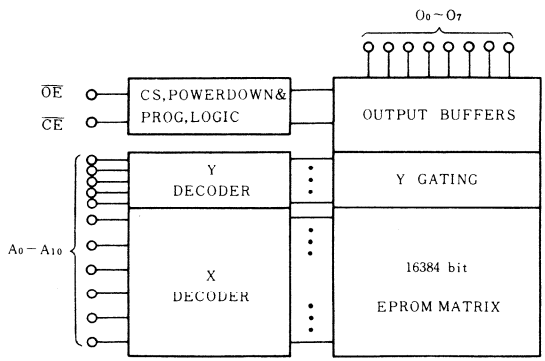
(DC-24C)

HN462716G

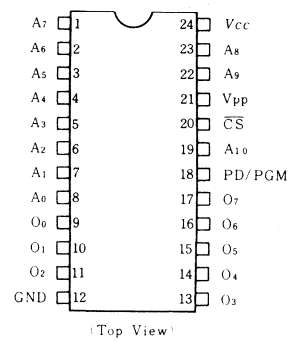


(DG-24B)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ PROGRAMMING OPERATION

Mode \ Pins	PD/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9~11, 13~17)
Read	V_{IL}	V_{IL}	+5	+5	Dout
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Power Down	V_{IL}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	Din
Program Verify	V_{IL}	V_{IL}	+25	+5	Dout
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	℃
Storage Temperature Range	T_{stg}	−65 to +125	℃
All Input and Output Voltages*	V_{IN}, V_{OUT}	−0.3 to +7	V
V_{PP} Supply Voltage*	V_{PP}	−0.3 to +28	V

* with respect to Ground

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V± 5%, V_{PP}=V_{CC}±0.6V)

Item	Symbol	Test Condition	min.	typ.	max.	Unit.
Input Leakege Curreut	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=5.25V/0.4V	—	—	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=5.85V	—	—	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$=V_{IH}, $\overline{OE}$=V_{IL}	—	21	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{OE}$=$\overline{CE}$=V_{IL}	—	62	100	mA
Input LowVoltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

Note: Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.

• AC CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address to Output Delay	t_{ACC}	$\overline{OE}$=$\overline{CE}$=V_{IL}	—	—	450	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$=V_{IL}	—	—	450	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$=V_{IL}	—	—	120	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$=V_{IL}	0	—	100	ns
Address to Output Hold	t_{OH}	$\overline{OE}$−$\overline{CE}$−V_{IL}	0	—	—	ns

• CAPACITANCE (Ta=25℃, f=1MHz)

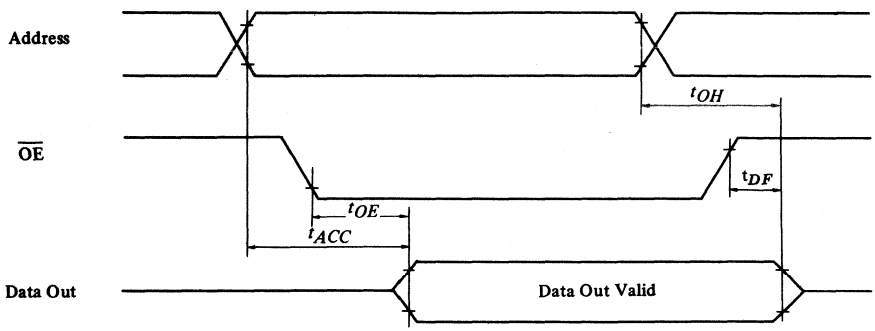
Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{IN}=0V	—	6	pF
Output Capacitance	C_{out}	V_{OUT}=0V	—	12	pF

• SWITCHING CHARACTERISTICS

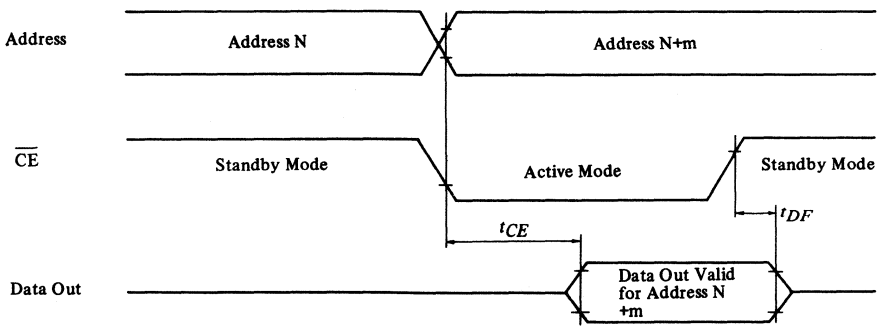
Test Conditions

Input Pulse Levels: 0.8V to 2.2V
Input Rise and Fall Times: ≤ 20 ns
Output Load: 1TTL Gate + 100 pF
Reference Level for Measuring Timing:
Inputs 1V and 2V
Outputs 0.8V and 2V

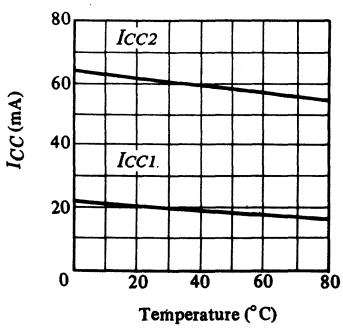
READ MODE ($\overline{CE}$ = V_{IL})

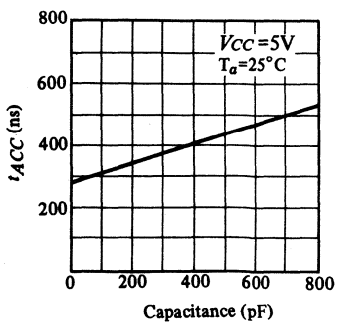


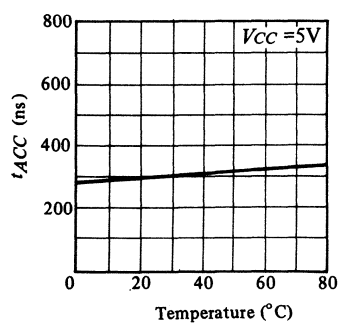
STANDBY MODE ($\overline{OE}$ = V_{IL})



• TYPICAL CHARACTERISTICS







• D.C. PROGRAMMING CHARACTERISTICS (Ta=25℃ ±5℃, V_{CC}=5V±5%, V_{PP}=25V±1V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{CC}=5.25V/0.4V	—	—	10	μA
V_{PP} Supply Current	I_{PP1}	$\overline{CE}=V_{IL}$	—	—	6	mA
V_{PP} Supply Current During Programming	I_{PP2}	$\overline{CE}=V_{IH}$	—	—	30	mA
V_{CC} Supply Current	I_{CC}		—	—	100	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	V_{CC}+1	V

• A.C. PROGRAMMING CHARACTERISTICS (Ta=25℃ ±5℃, V_{CC}=5V±5%, V_{PP}=25V±1V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		2	—	—	μs
$\overline{OE}$ Hold Time	t_{OEH}		5	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}	$\overline{CE}=V_{IL}$	0	—	120	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$	—	—	120	ns
Program Pulse Width	t_{PW}		45	50	55	ms
Program Pulse Rise Time	t_{PRT}		5	—	—	ns
Program Pulse Fall Time	t_{PFT}		5	—	—	ns

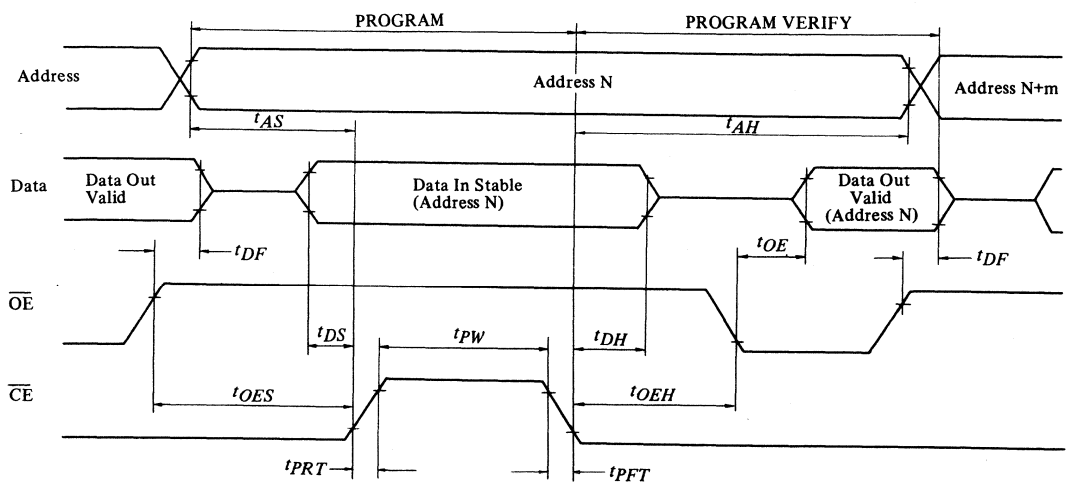
Note: V_{CC} must be applied simultaneously or before V_{pp} and removed simultaneously or after V_{pp}.

• SWITCHING CHARACTERISTICS

Test Conditions
Input Pulse Level: 0.8V to 2.2V
Input Rise and Fall Times: ≤ 20 ns

Output Load: 1 TTL Gate + 100 pF
Reference Level for Measuring Timing:
Inputs; 1V and 2V, Outputs; 0.8V and 2V

• PROGRAMMING WAVEFORMS



ERASE

Erasure of HN462716 is performed by exposure to ultraviolet light with a wavelength of 2537Å, and all the output data are ıanged to "1" after this erasure procedure.

The minimum integrated close (i.e., UV intensity x exposure time) for erasure is 15W · sec/cm^2.

DEVICE OPERATION

READ MODE

ataout is available 450 ns (t_{ACC}) from addresses with $\overline{OE}$ w or 120 ns (t_{OE}) from $\overline{OE}$ with addresses stable.

DESELECT MODE

ıe outputs may be OR-tied together with the other HN-32716s. When HN462716s are deselected, the $\overline{OE}$ inputs ust be at high TTL level.

POWER DOWN MODE

ɔwer down is achieved with $\overline{CE}$ high TTL level. In this ode the outputs are in a high impedance state.

PROGRAMMING

ıitially, and after each erasure, all bits of the HN462716 e in the "high" state (Output High). Data is introduced / selectively programming "low" into the desired bit loca-ɔns. In the programming mode, Vpp power supply is at 5V and $\overline{OE}$ input is at high TTL level. Data to be pro-ammed are presented 8-bits in parallel, to the data output ıes (O1 to O8).

The addresses and inputs are at TTL levels.

After the address and data setup, a 50 ms, active high program pulse is applied to the $\overline{CE}$ input. The $\overline{CE}$ is at TTL level.

The HN462716 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

• PROGRAM VERIFY

The HN462716 has a program verify mode. A verify should be performed on the programmed bits to determine that they were correctly programmed. In this mode Vpp is at 25V.

• PROGRAM INHIBIT

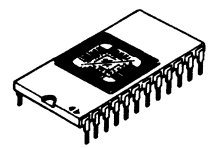
Programming of multiple HN462716s in parallel with different data is easily accomplished by using this mode. Except for $\overline{CE}$, all like inputs of the parallel HN462716s may be common.

A TTL program pulse applied to 0 HN462716's $\overline{CE}$ input will program that HN462716. A low level $\overline{CE}$ inhibits the other HN462716s from being programmed.

HN462532

4096-word X 8-bit UV Erasable and Programmable Read Only Memory

The HN462532 is a 4096 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

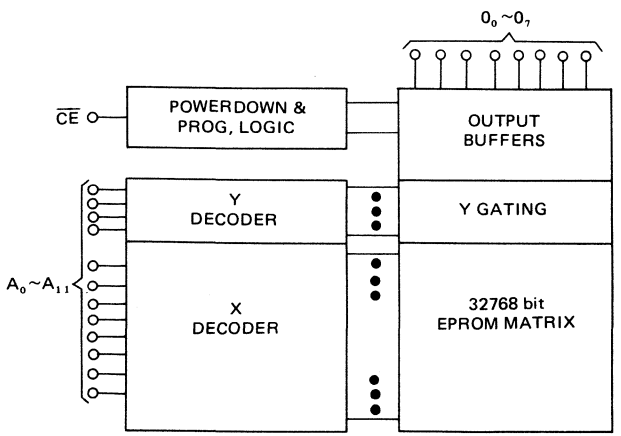


(DC-24C)

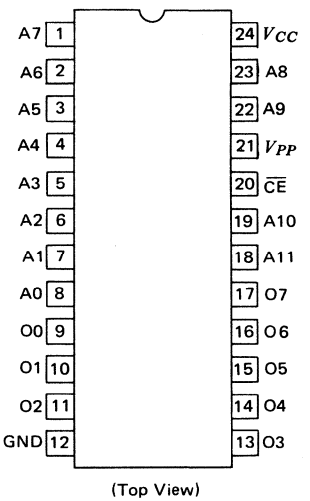
■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- Simple Programming . . . . . Program Voltage: +25V D.C.
  Program with One 50ms Pulse
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-Chip Address Decode
- Access Time . . . . . 450ns (Max.)
- Low Power Dissipation . . . . . 858mW (Max.) Active Power
  201mW (Max.) Standby Power
- Three State Output . . . . . OR-Tie Capability
- Compatible with TMS2532

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HITACHI

MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9to11, 13to17)
Read	V_{IL}	+5	+5	Dout
Stand by	V_{IH}	+5	+5	High Z
Program	Pulsed V_{IH} to V_{IL}	+25	+5	Din
Program Inhibit	V_{IH}	+25	+5	High Z

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltages*	V_{IN}, V_{out}	−0.3 to +7	V
Vpp Voltage*	V_{PP}	−0.3 to +28	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C

with respect to GND.

READ OPERATION

D.C. AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%, V_{PP} = V_{CC} ±0.6V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in} = 5.25 V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25 V / 0.4 V	—	—	10	μA
Vpp Current	I_{PP1}	V_{PP} = 5.85 V	—	—	12	mA
Vcc Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	—	—	25	mA
Vcc Current (Active)	I_{CC2}	$\overline{CE}$ = V_{IL}	—	—	150	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −400μA	2.4	—	—	V

otes: Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.

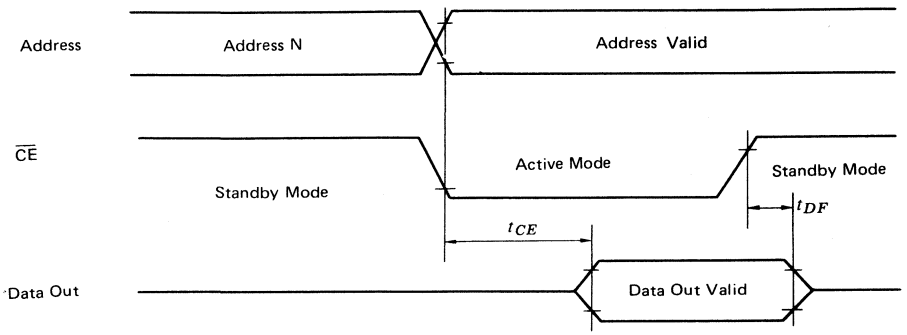
AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%, V_{PP} = V_{CC} ±0.6V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address to Output Delay	t_{ACC}	$\overline{CE}$ = V_{IL}	—	—	450	ns
$\overline{CE}$ to Output Delay	t_{CE}		—	—	450	ns
$\overline{CE}$ High to Output Float	t_{DF}		0	—	100	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = V_{IL}	0	—	—	ns

• SWITCHING CHARACTERISTICS

Test Conditions

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Times:	≤20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V, Outputs; 0.8V and 2V



• CAPACITANCE (T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	12	pF

■ PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 5V ±5%, V_{PP} = 25V ±1V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in} = 5.25V / 0.4V	–	–	10	μA
V_{PP} Supply Current During Programming	I_{PP2}	$\overline{CE}$ = V_{IL}	–	–	30	mA
V_{CC} Supply Current	I_{CC}		–	–	150	mA
Input Low Level	V_{IL}		–0.1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{CC}+1	V

AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 5V ±5%, V_{PP} = 25V ±1V)

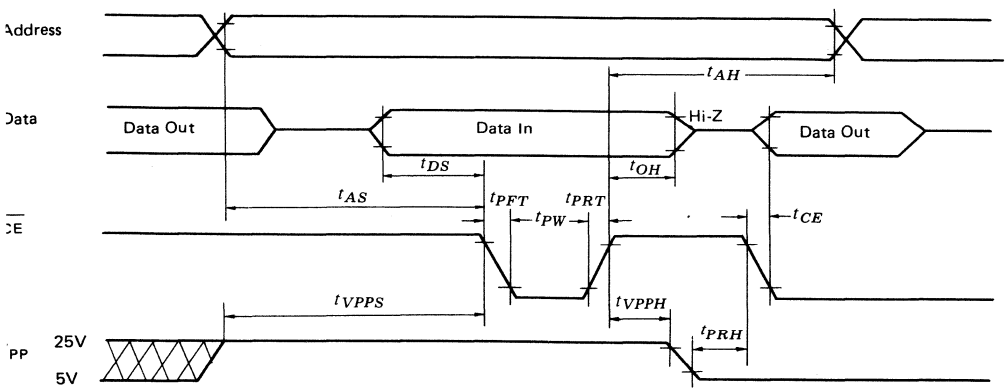
Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		2	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
Setup Time from V_{PP}	t_{VPPS}		0	–	–	ns
Program Pulse Hold Time	t_{PRH}		0	–	–	ns
V_{PP} Hold Time	t_{VPPH}		0	–	–	ns
Program Pulse Width	t_{PW}		45	50	55	ms
Program Pulse Time	t_{PRT}		5	–	–	ns
Program Pulse Time	t_{PFT}		5	–	–	ns

Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

SWITCHING CHARACTERISTICS

Test Conditions

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Times:	≤20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V, Outputs; 0.8V and 2V



ERASE

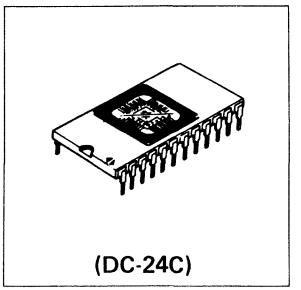
Erasure of HN462532 is performed by exposure to ultraviolet light with a wavelength of 2537Å, and all the output data are changed to "1" after this erasure procedure.

The minimum integrated close (i.e.,UV intensity x exposure time) for erasure is 15W· sec/cm^2.

HN462732

4096-word × 8-bit UV Erasable and Programmable Read Only Memory

The HN462732 is a 4096 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

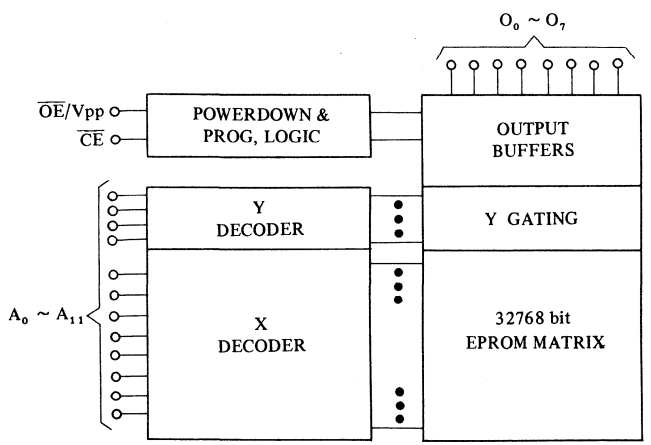


(DC-24C)

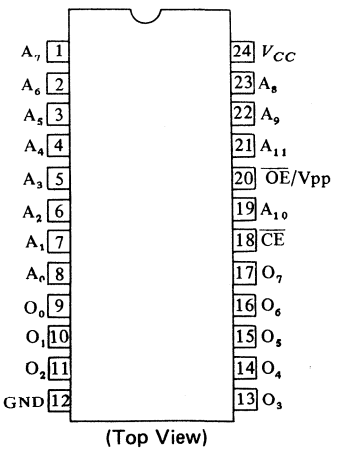
■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- Simple Programming . . . . . Program Voltage: +25V D.C.
  Program with One 50ms Pulse
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-Chip Address Decode
- Access Time . . . . . 450ns Max.
- Low Power Dissipation . . . . . 150mA Max. Active Current
  30mA Max. Standby Current
- Three State Output . . . . . OR-Tie-Capability
- Compatible with INTEL 2732

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HITACHI

■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9 ~ 11, 13 ~ 17)
Read	V_{IL}	V_{IL}	+5	Dout
Stand by	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	Din
Program Verify	V_{IL}	V_{IL}	+5	Dout
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to + 70	°C
Storage Temperature Range	T_{stg}	−65 to + 125	°C
All Input and Output Voltages*	V_{IN}, V_{out}	−0.3 to + 7	V
V_{PP} Voltage*	$\overline{OE}/V_{PP}$	−0.3 to +28	V

*with respect to GND

■ READ OPERATION

• D. C. AND OPERATING CHARACTERISTICS (T_a=0 to +70°C, V_{CC}=5V±5%)

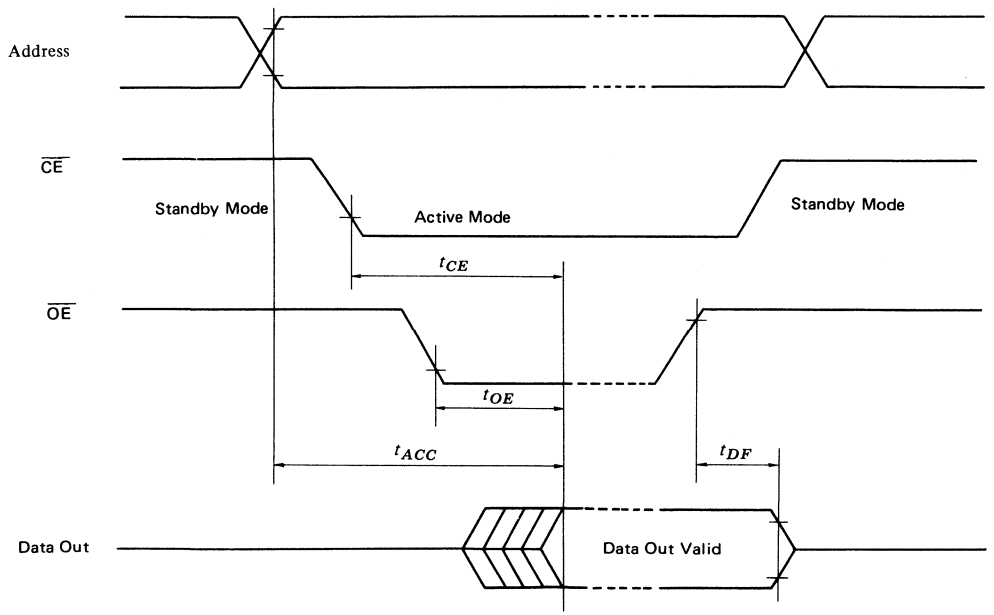
Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current (Except $\overline{OE}/V_{PP}$)	I_{LI1}	V_{IN} = 5.25 V	–	–	10	μA
$\overline{OE}/V_{PP}$ Input Leakage Current	I_{LI2}	V_{IN} = 5.25 V	–	–	300	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25 V	–	–	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	–	–	30	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	–	–	150	mA
Input Low Voltage	V_{IL}		−0.1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC} + 1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V

• A. C. CHARACTERISTICS (T_a=0 to +70°C, V_{CC}=5V±5%)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	–	450	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	–	450	ns
Output Enable to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	–	120	ns
Output Enable High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	–	100	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	–	ns

• SWITCHING CHARACTERISTICS

Test Condition
Input Pulse Levels: 0.8V to 2.2V
Input Rise and Fall Times: ≤20ns
Output Load: 1TTL Gate + 100pF
Reference Level for Measuring Timing: Inputs 1V and 2V
Outputs 0.8V and 2V



• **CAPACITANCE** (T_a=25°C, f=1 MHz)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Capacitance (Except $\overline{OE}/V_{PP}$)	C_{IN1}	V_{IN} = 0 V	–	–	6	pF
$\overline{OE}/V_{PP}$ Input Capacitance	C_{IN2}	V_{IN} = 0 V	–	–	20	pF
Output Capacitance	C_{out}	V_{out} = 0 V	–	–	12	pF

■ PROGRAMMING OPERATION

• D.C. PROGRAMMING CHARACTERISTICS (V_{CC}=5V±5%, V_{pp}=25V±1V, T_a=25°C±5°C)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25/0.4 V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	V
Output High Voltage During Verify	V_{OH}	I_{OH} = –400 μA	2.4	–	–	V
V_{CC} Supply Current	I_{CC}		–	–	150	mA
Input Low Level	V_{IL}		–0.1	–	0.8	V
Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)	V_{IH}		2.0	–	V_{CC} + 1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{PP}	–	–	30	mA

• A.C. PROGRAMMING CHARACTERISTICS (V_{CC}=5V±5%, V_{pp}=25V±1V, T_a=25°C±5°C)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
Chip Enable to Output Float Delay	t_{DF}		0	–	120	ns
Data Valid from $\overline{CE}$	t_{DV}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}	–	–	1	μs
$\overline{CE}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{OE}$ Pulse Rise Time During Programming	t_{PRT}		50	–	–	ns
V_{PP} Recovery Time	t_{VR}		2	–	–	μs

• SWITCHING CHARACTERISTICS

Test Conditions

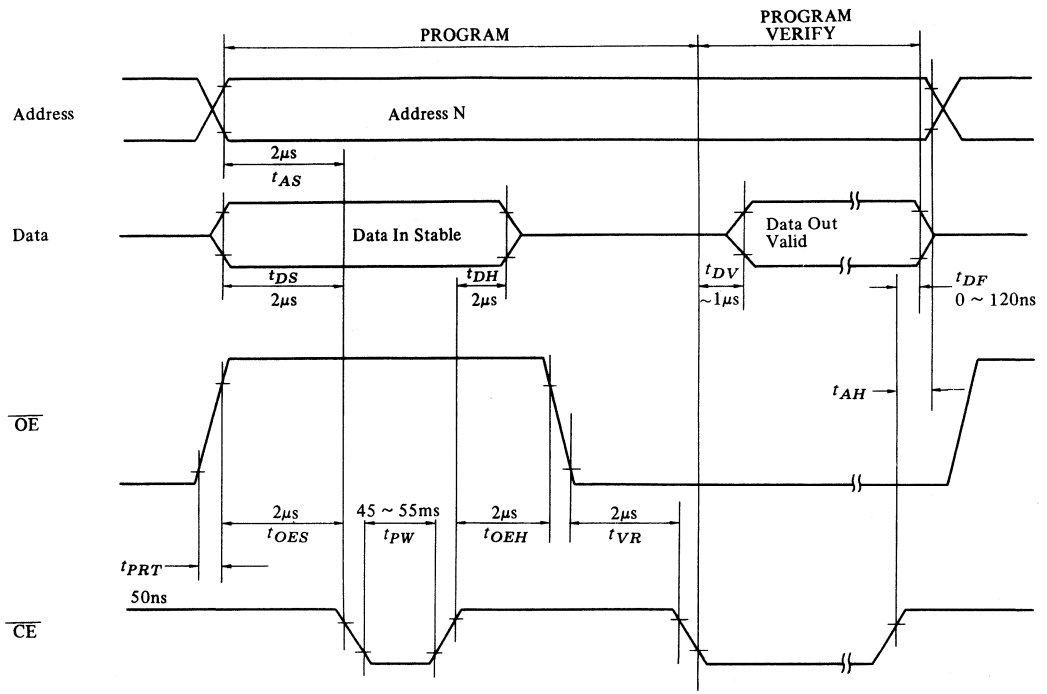
Input Pulse Level: 0.8V to 2.2V

Input Rise and Fall Times: ≤20ns

Output Load: 1 TTL Gate + 100pF

Reference Level for Measuring Timing: Inputs; 1V and 2V,
Outputs; 0.8V and 2V

- PROGRAMMING WAVE FORMS



- **ERASE**

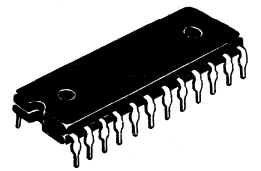
Erasure of HN462732 is performed by exposure to Ultraviolet light of 2537Å, and all the output data are changed to "1" after this prosedure.

The minimum integrated close (i.e., UV intensity x exposure time) for erasure is 15W · sec/cm^2.

HN48016P

2048-word X 8-bit Electrically Erasable and Programmable ROM

This device operates from a single power supply and features fast single address location programming. All the words are erased by one TTL level pulse. Erasing the bit pattern and programming new pattern can be made within 22 seconds.

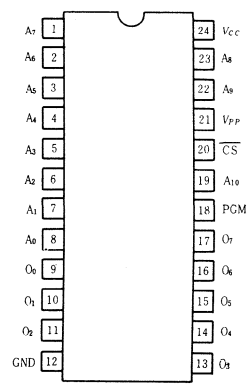


(DP-24)

FEATURES

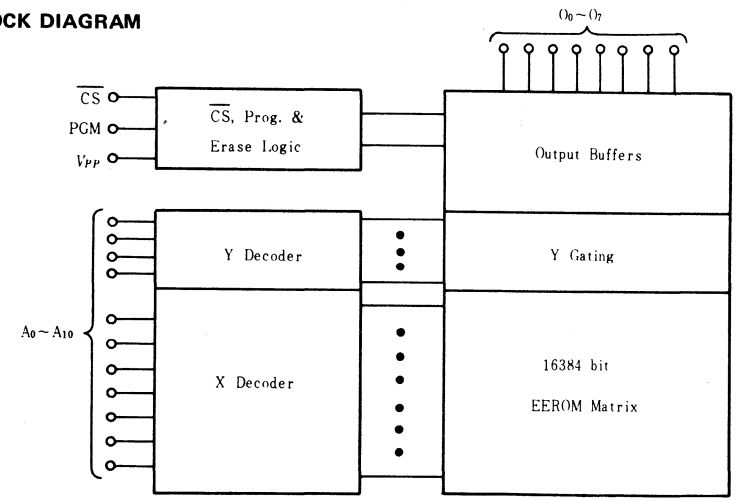
- Single Power Supply ..... +5V±5%
- Simple Programming ..... Program voltage: +25V DC. Program with one 10ms pulse.
- Electrically Erasing ..... Erase Voltage: +25V DC. Erase all words with one 1sec pulse.
- Fully Static ..... No clocks required.
- Inputs and Outputs TTL compative during read, program and erase mode.
- Fully Decoded ..... On-Chip Address Decode.
- Access Time ..... 350ns Max.
- Low Power Dissipation ..... 300mW Max.
- Three State Output ..... OR-Tie Capability
- Pin-out Compatible with Intel 2716.

■ PIN ARRANGEMENT



(Top View)

BLOCK DIAGRAM



MODE SELECTION

Mode \ Pins	PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (8~11, 13~17)
READ	V_{IL}	V_{IL}	+5	+5	D_{OUT}
DESELECT	Don't Care	V_{IH}	+5	+5	High Z
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	+25	+5	D_{OUT}
ERASE	Pulsed V_{IL} to V_{IH}	V_{IL}	+25	+5	

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
All Inputs and Output Voltage	V_{IN}, V_{out}	−0.3 to V_{CC} + 0.3 or V_{PP} + 0.3	V
V_{CC} Voltage	V_{CC}	−0.3 to +7.0	V
V_{PP} Voltage	V_{PP}	−0.3 to +28	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C

■ READ OPERATION

- **DC and Operating Characteristics** (V_{CC} = 5V±5%, V_{PP} = V_{CC}±0.6V*, T_a = 0 to +70°C)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Current	I_{CC1}	$\overline{CS}$ = V_{IH}/V_{IL}	–	32	50	mA
V_{PP} Current	I_{PP1}	V_{PP} = 5.85V	–	4	7	mA
Input Voltage	V_{IL}		−0.1	–	0.8	V
	V_{IH}		2.0	–	–	V
Output Voltage	V_{OL}	I_{OL} = 1.6mA	–	–	0.4	V
	V_{OH}	I_{OH} = −100 μA	2.4	–	–	– V

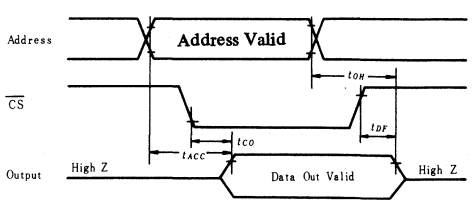
* The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.

- **AC Characteristics** (V_{CC} = 5V±5%, V_{PP} = V_{CC} ±0.6V, T_a = 0 to +70°C)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address to Output Delay	t_{ACC}	PGM = CS = V_{IL}	–	200	350	ns
Chip Select to Output Delay	t_{CO}	PGM = V_{IL}	–	70	150	ns
Chip Deselect to Output Float	t_{DF}		0	40	100	ns
Address to Output Hold	t_{OH}	PGM = CS = V_{IL}	10	–	–	ns

- **Test Condition**

Input pulse levels; 0.8V to 2.0V
Input rise and fall time; 20ns
Output load; 1TTL Gate + 100 pF
Reference level for Measuring Timing; Inputs 1V and 1.8V
Outputs 0.8V and 2.0V



- **Capacitance** (T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	–	7.5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	15	pF

■ PROGRAM OPERATION

- **DC Programming Characteristics** (V_{CC} = 5V±5%, V_{PP} = 25V±1V, T_a = 25°C±5°C)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
V_{CC} Supply Current	I_{CC2}		–	32	50	mA
V_{PP} Supply Current	I_{PP2}		–	10	20	mA
Input Voltage	V_{IL}		–0.1	–	0.8	V
	V_{IH}		2.0	–	–	V

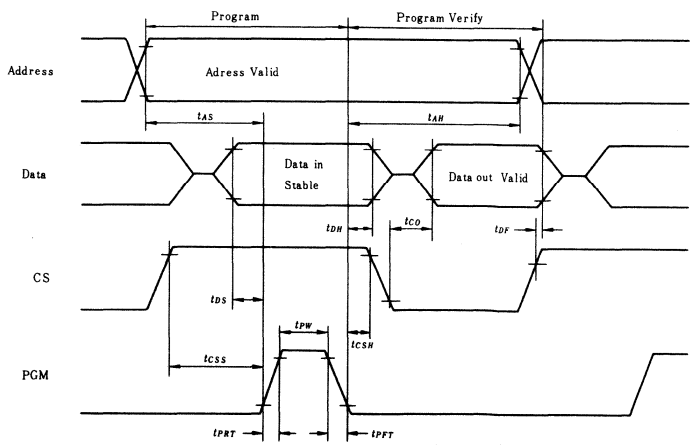
- **AC Programming Characteristics** (V_{CC} = 5V±5%, V_{PP} = 25V±1V, T_a = 25°C±5°C)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{CS}$ Setup Time	t_{CSS}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		2*	–	–	μs
$\overline{CS}$ Hold Time	t_{CSH}		7	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
Chip Deselect to Output Float Delay	t_{DF}		0	40	100	ns
Chip Select to Output Delay	t_{CO}		–	70	150	ns
Program Pulse Width	t_{PW}		10	–	–	ms
Program Pulse Rise Time	t_{PRT}		5	–	–	ns
Program Pulse Fall Time	t_{PFT}		5	–	–	ns

* If the mode changes from program mode to program verify mode sequentially (in the same address), t_{AH} must be larger than $t_{CSH} + t_{CO}$.

- **Test Condition**

nput pulse levels; 0.8V to 2.0V
nput rise and fall time; 20ns (10% to 90%)
Reference level for Measuring Timing; Input 1V and 1.8V
Output 0.8V and 2.0V



■ ERASE OPERATION

- **DC Erasing Characteristics** (V_{CC} = 5V±5%, V_{PP} = 25V±1V, T_a = 25°C±5°C)

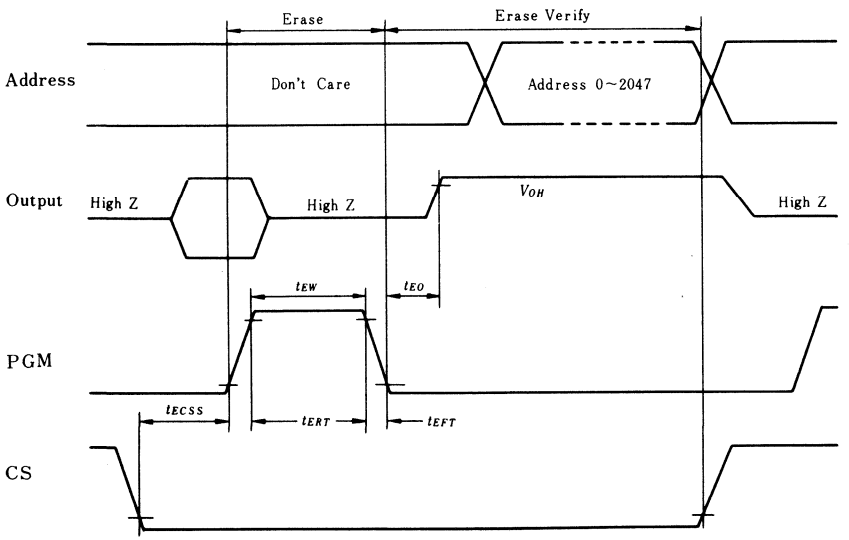
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
V_{CC} Supply Current	I_{CC3}		–	32	50	mA
V_{PP} Supply Current	I_{PP3}		–	10	20	mA
Input Voltage	V_{IL}		−0.1	–	0.8	V
	V_{IH}		2.0	–	–	V

- **AC Erasing Characteristics** (V_{CC} = 5V±5%, V_{PP} = 25V±1V, T_a = 25°C±5°C)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
CS Setup Time	t_{ECSS}		2	–	–	μs
PGM to Output Delay	t_{EO}		7	–	–	μs
Erase Pulse Width	t_{EW}		1000	–	–	ms
Erase Pulse Rise Time	t_{ERT}		5	–	–	ns
Erase Pulse Fall Time	t_{EFT}		5	–	–	ns

- **Test Condition**

Input pulse levels; 0.8V to 2.0V
Input rise and fall time; 20ns (10% to 90%)
Reference level for Measuring Timing; Input 1V and 1.8V
Output 0.8V and 2.0V



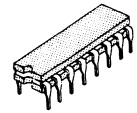
BIPOLAR RAM

HM2105

256-word × 1-bit Fully Decoded Random Access Memory

The HM2105 is a 256-word x 1-bit read/write random access memory developed for application to buffer memory, control memory, etc.

- Level . . . . . 10K ECL compatible
- Chip select access time . . . . . 12ns (max)
- Address access Time . . . . . 35ns (max)
- Power Consumption . . . . . 1.8mW/bit (typ)
- Output obtainable by Wired-OR (open emitter)



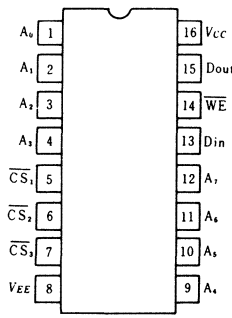
(DG-16)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
any one H	×	×	L	Not Selected
all L	L	L	L	Write "0"
all L	L	H	L	Write "1"
all L	H	×	Dout *	Read

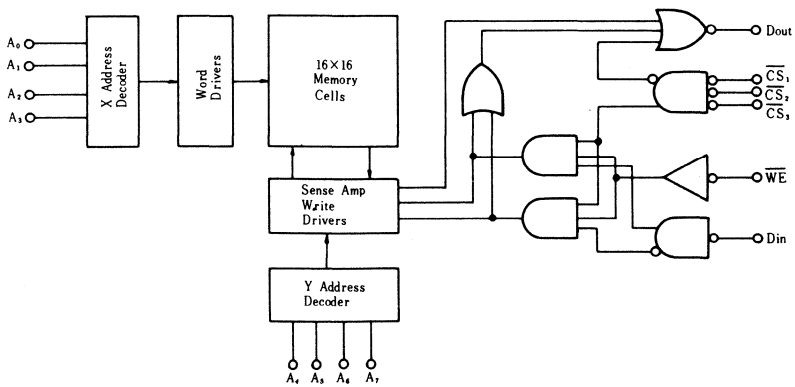
× : Don't care
* : Read out non-inverted

■ PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



HITACHI

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2105	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	$Iout$	−30	mA
Storage Temperature	$Tstg$	−65 to +150	°C
Storage Temperature	$Tstg$ (Bias) *	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min. (B)	typ.	max. (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	− 840	mV
			+25°C	− 960	—	− 810	
			+75°C	− 900	—	− 720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	− 980	—	—	
			+75°C	− 920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	− 840	mV
			+25°C	−1105	—	− 810	
			+75°C	−1045	—	− 720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Power Supply Current	I_{EE}	All Input and Output Open. Test pin 8.	+75°C	− 120	−85	—	mA
			0°C	− 130	−95	—	

●AC CHARACTERISTICS (V_{EE} = −5.2V ± 5%, Ta = 0 to +75°C, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Chip Select Access Time	t_{ACS}		—	7	12	ns
Chip Select Recovery Time	t_{RCS}		—	7	12	ns
Address Access Time	t_{AA}		—	20	35	ns

2. WRITE MODE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Write Pulse Width	t_W	t_{WSA} = 8ns	25	15	—	ns
Data Setup Time	t_{WSD}		5	3	—	ns
Data Hold Time	t_{WHD}		5	3	—	ns
Address Setup Time	t_{WSA}	t_W = 25ns	8	5	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Chip Select Setup Time	t_{WSCS}		5	3	—	ns
Chip Select Hold Time	t_{WHCS}		5	3	—	ns
Write Disable Time	t_{WS}		3	14	—	ns
Write Recovery Time	t_{WR}		—	15	20	ns

3. RISE AND FALL TIME

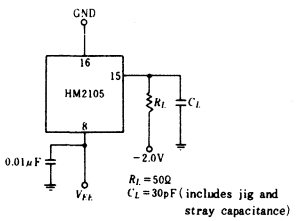
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Output Rise Time	t_r		—	5	—	ns
Output Fall Time	t_f		—	5	—	ns

4. CAPACITANCE

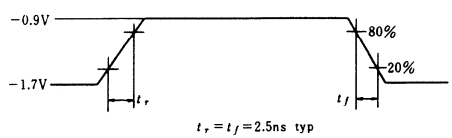
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Lead Capacitance	*Cin*		—	4	5	pF
Output Lead Capacitance	*Cout*		—	7	8	pF

■TEST CIRCUIT AND WAVEFORMS

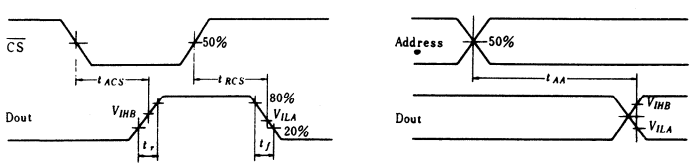
1. LOADING CONDITION



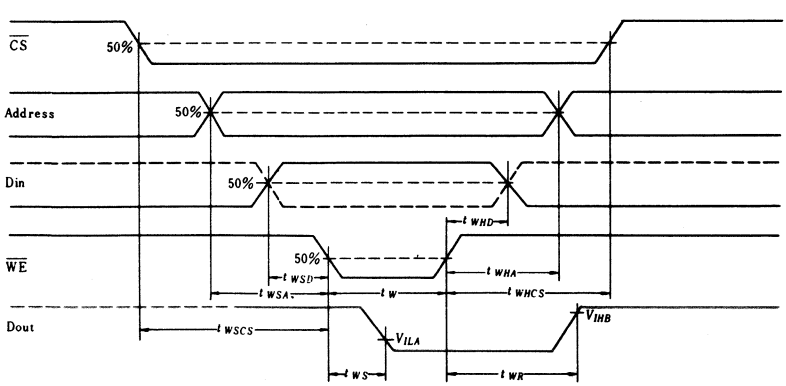
2. INPUT PULSE



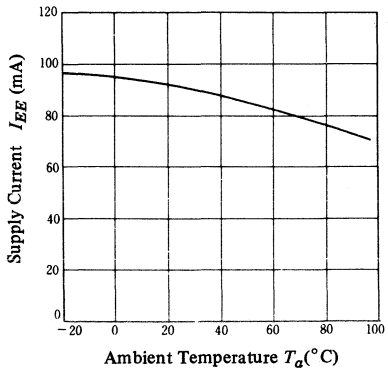
3. READ MODE



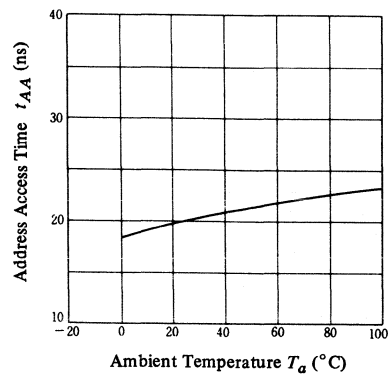
4. WRITE MODE



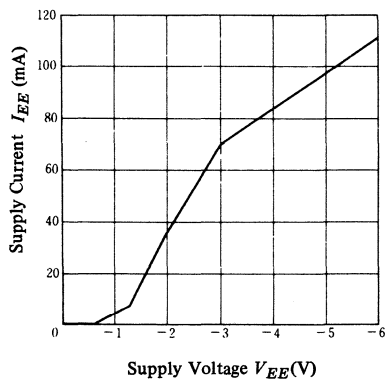
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

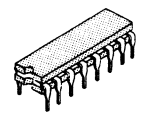


HM2106

256-word × 1-bit Fully Decoded Random Access Memory

The HM2106 is an ECL compatible, 256-word x 1-bit, read/write, random access memory developed for application to scratch pad, control and buffer memories, etc. whitch require high speeds.

- It is compatible with 10K ECL logic.
- Chip select access time . . . . . 10ns (max)
- Address Access time . . . . . 15ns (max)
- Power consumption . . . . . 1.8mW/bit (typ)
- Output obtainable by wired-OR (open emitter)



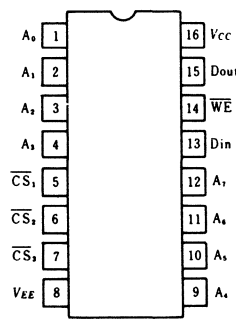
(DG-16)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
any one H	×	×	L	Not Selected
all L	L	L	L	Write "0"
all L	L	H	L	Write "1"
all L	H	×	Dout *	Read

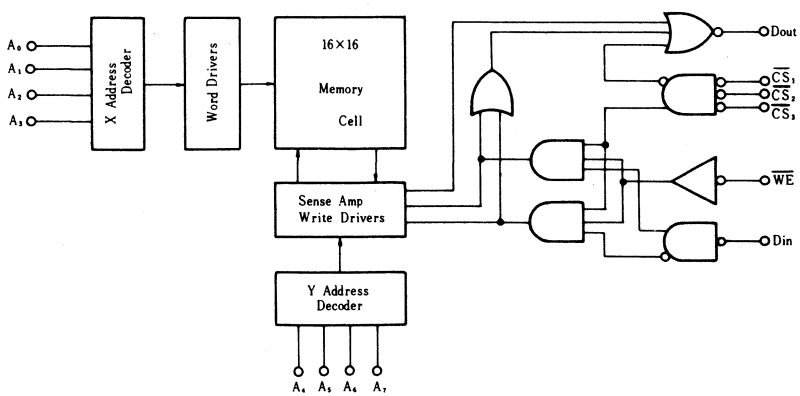
× : Don't care
* : Read out non-inverted

■ PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2106	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	*Vin*	+0.5 to V_{EE}	V
Output Current	*Iout*	−30	mA
Storage Temperature	*Tstg*	−65 to +150	°C
Storage Temperature	*Tstg* (Bias) *	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min.(B)	typ.	max.(A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / V_{IN} = V_{ILB}	0 to +75°C	0.5	—	170	
		Other		−50	—		
Supply Current	I_{EE}	All Input and Output Open. Test pin 8	+75°C	−120	−85		mA
			0°C	−130	−95		

●AC CHARACTERISTICS (V_{EE} = −5.2V ± 5%, Ta = 0 to +75°C, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Chip Select Access Time	t_{ACS}		—	6	10	ns
Chip Select Recovery Time	t_{RCS}		—	6	10	ns
Address Access Time	t_{AA}		3	9	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	10	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W = 10ns	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		3	—	—	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

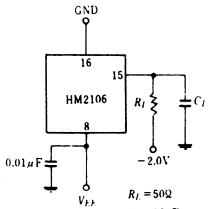
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Output Rise Time	t_r		—	3	—	ns
Output Fall Time	t_f		—	3	—	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	*Cin*		—	2	5	pF
Output Capacitance	*Cout*		—	3	8	pF

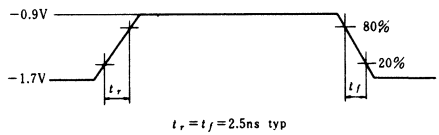
■TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION



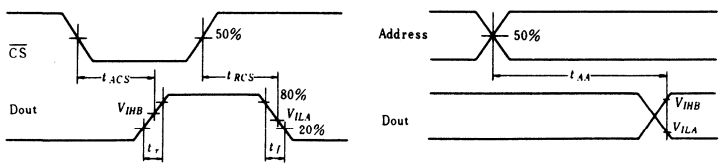
$R_l = 50\Omega$
$C_l = 30pF$ (includes jig and stray capacitance)

2. INPUT PULSE

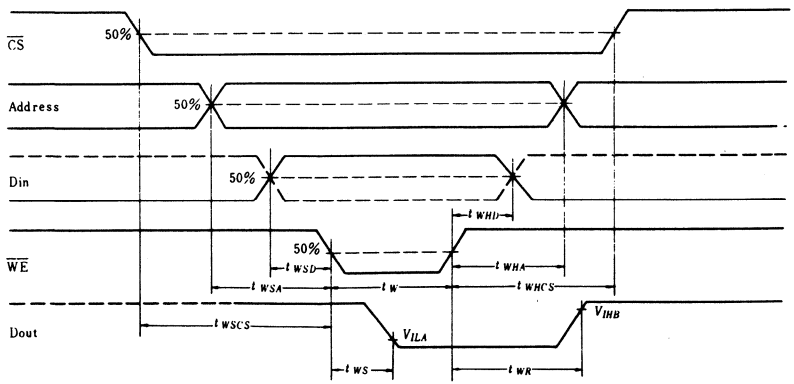


$t_r = t_f = 2.5ns$ typ

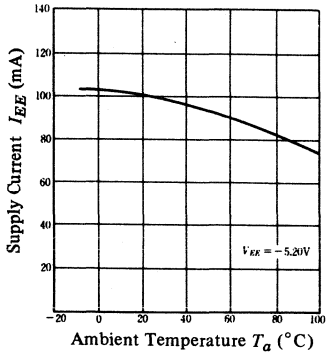
3. READ MODE



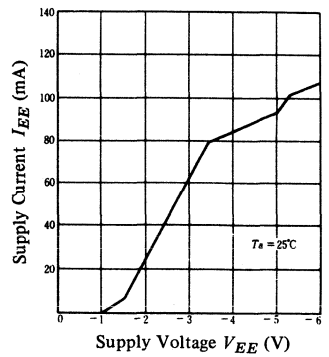
4. WRITE MODE



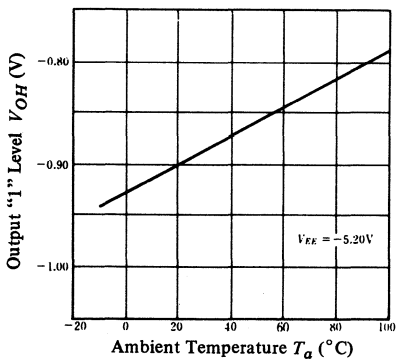
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



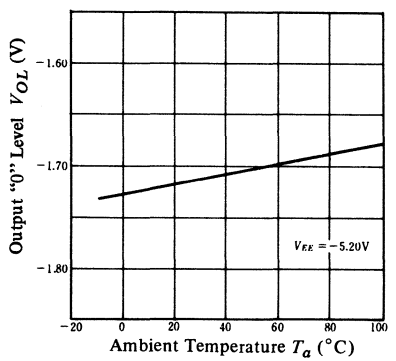
SUPPLY CURRENT vs. SUPPLY VOLTAGE



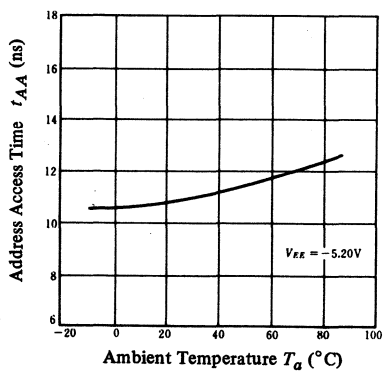
OUTPUT "1" LEVEL vs. AMBIENT TEMPERATURE



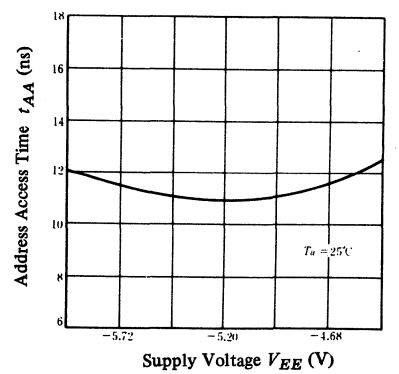
OUTPUT "0" LEVEL vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



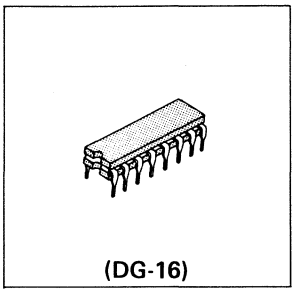
256-word × 1-bit Fully Decoded Random Access Memory

The HM10414 is ECL 10K compatible, 256-word x 1-bit, read/write, random access memory developed for high speed systems such as scratch pad and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

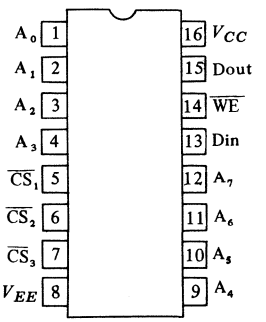
The HM10414 is encapsulated in cerdip-16pin package, compatible with Fairchild's F10414.

- Fully compatible with 10K ECL level
- Address access time; HM10414: 10ns (max.)
  HM10414-1: 8ns (max.)
- Write pulse width: 6ns (min.)
- Three chip select pins
- Output obtainable by wired-OR (open emitter)



(DG-16)

■ PIN ARRANGEMENT



(Top View)

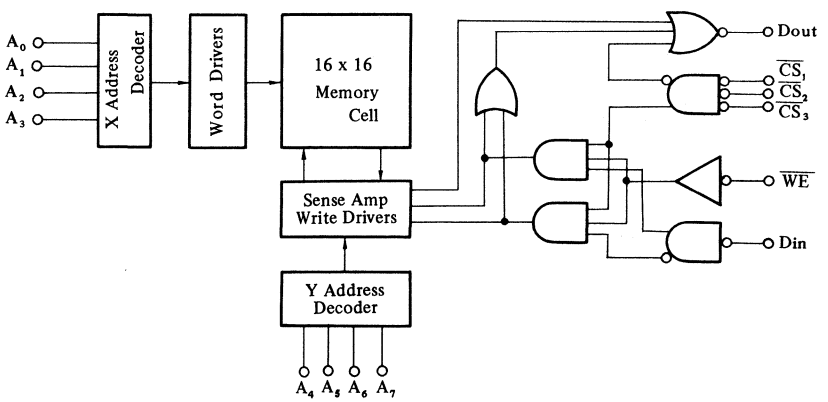
■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
any one H	×	×	L	Not Selected
all L	L	L	L	Write "0"
all L	L	H	L	Write "1"
all L	H	×	Dout*	Read

× : Don't care

* : Read out non-inverted

■ BLOCK DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{EE} = −5.2 V, R_L = 50 Ω to −2.0 V, T_a=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min. (B)	typ.	max. (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	–	−840	mV
			+25°C	−960	–	−810	
			+75°C	−900	–	−720	
	V_{OL}		0°C	−1870	–	−1665	
			+25°C	−1850	–	−1650	
			+75°C	−1830	–	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	–	–	mV
			+25°C	−980	–	–	
			+75°C	−920	–	–	
	V_{OLC}		0°C	–	–	−1645	
			+25°C	–	–	−1630	
			+75°C	–	–	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	–	−840	mV
			+25°C	−1105	–	−810	
			+75°C	−1045	–	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	–	−1490	
			+25°C	−1850	–	−1475	
			+75°C	−1830	–	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	–	–	220	μA
	I_{IL}	$\overline{CS}$	V_{IN} = V_{ILB} 0 to +75°C	0.5	–	170	
		Other		−50	–	–	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	+75°C	–	−130	–	mA
			0°C	−180	−140	–	

• AC CHARACTERISTICS (V_{EE}=−5.2V±5%, T_a=0 to + 75°C, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM10414			HM10414-1			Unit
			min.	typ.	max.	min.	typ.	max.	
Chip Select Access Time	t_{ACS}		–	3	6	–	3	6	ns
Chip Select Recovery Time	t_{RCS}		–	3	6	–	3	6	ns
Address Access Time	t_{AA}		–	7	10	–	6	8	ns

2. WRITE MODE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Write Pulse Width	t_W	t_{WSA} = 2 ns	6	4	–	ns
Data Setup Time	t_{WSD}		1	0	–	ns
Data Hold Time	t_{WHD}		1	0	–	ns
Address Setup Time	t_{WSA}	t_W = 6 ns	2	0	–	ns
Address Hold Time	t_{WHA}		2	0	–	ns
Chip Select Setup Time	t_{WSCS}		1	0	–	ns
Chip Select Hold Time	t_{WHCS}		1	0	–	ns
Write Disable Time	t_{WS}		–	–	5	ns
Write Recovery Time	t_{WR}		–	–	5	ns

3. RISE/FALL TIME

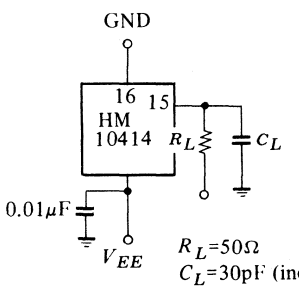
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Output Rise Time	t_r		–	1.5	2.5	ns
Output Fall Time	t_f		–	1.5	2.5	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}		–	3	5	pF
Output Capacitance	C_{out}		–	5	8	pF

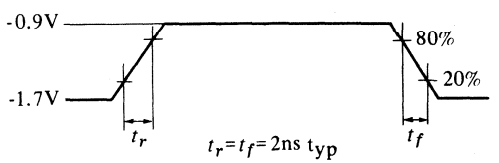
■ TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITIONS

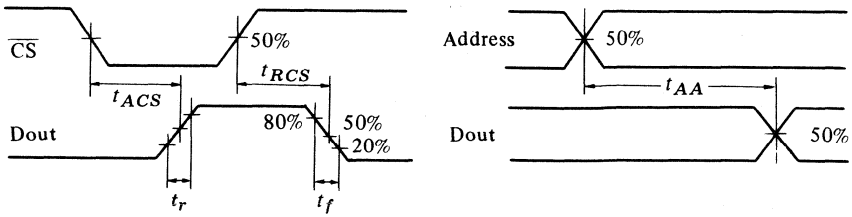


R_L=50Ω
C_L=30pF (includes jig and stray capacitance)

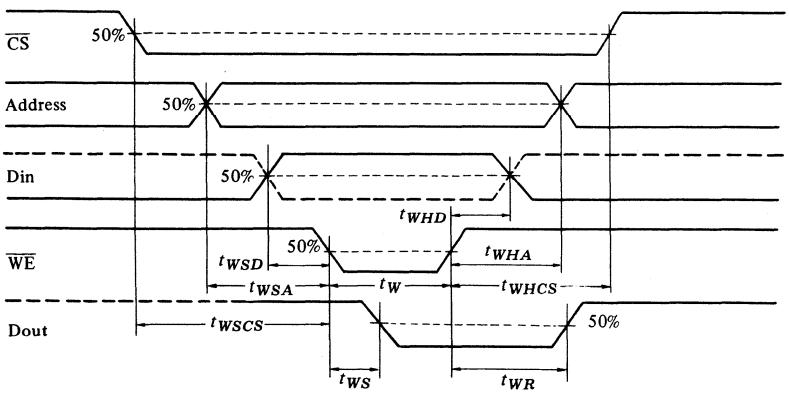
2. INPUT PULSE



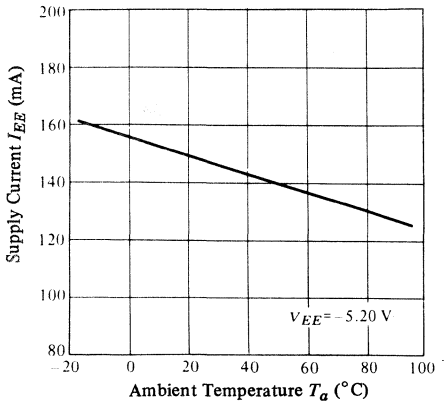
3. READ MODE



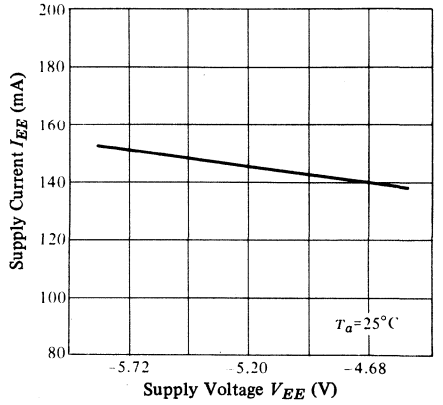
4. WRITE MODE



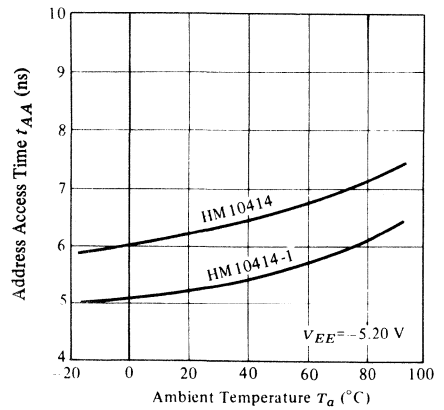
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



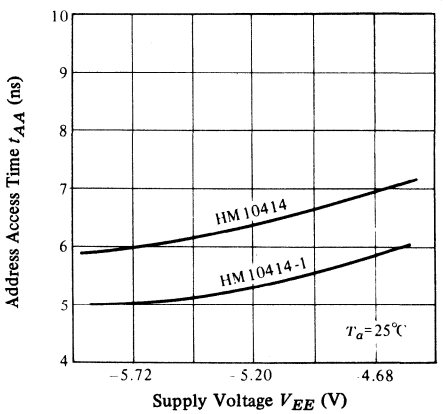
SUPPLY CURRENT VS. SUPPLY VOLTAGE



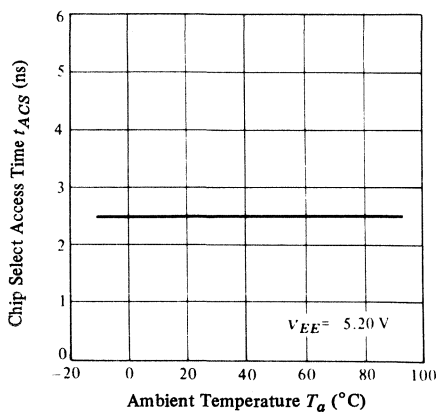
ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



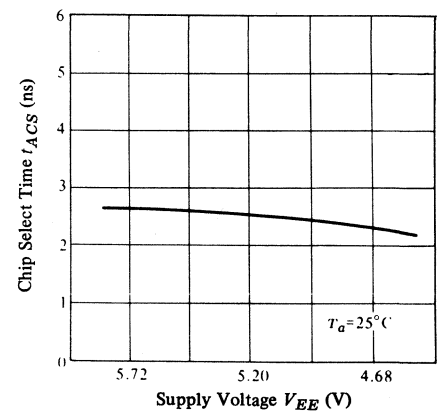
ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE



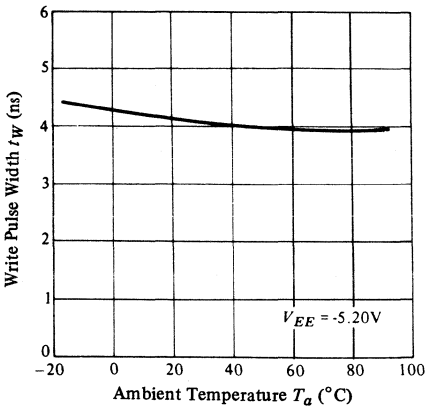
CHIP SELECT ACCESS TIME VS. AMBIENT TEMPERATURE



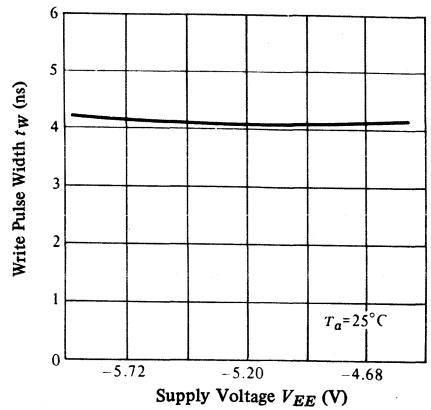
CHIP SELECT ACCESS TIME VS. SUPPLY VOLTAGE



WRITE PULSE WIDTH VS. AMBIENT TEMPERATURE



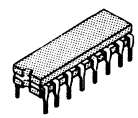
WRITE PULSE WIDTH VS. SUPPLY VOLTAGE



HM2110,HM2110-1, HM2110-2

The HM2110 Series item is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

- It is compatible with 10K ECL logic.
- Chip select access time . . . . . 10ns (max.)
- Address access time . . . . . HM2110: 35ns (max.)
  HM2110-1: 25ns (max.)
  HM2110-2: 20ns (max.)
- Power consumption . . . . . 0.5mW/bit (typ)
- Output obtainable by Wired-OR (open emitter).



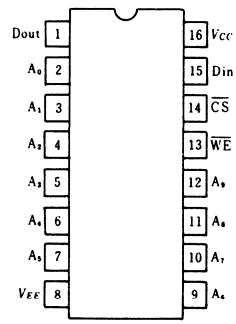
(DG-16A)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

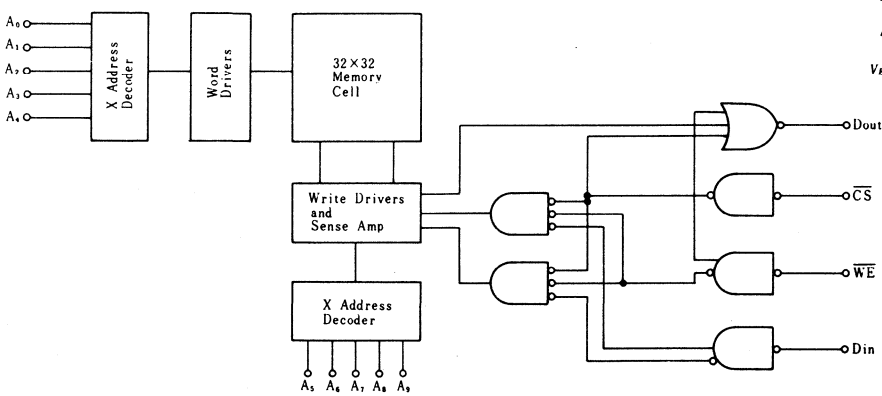
× : irrelevant
* : Read out noninverted

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXMUM RATINGS

Item	Symbol	HM2110 Series	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	*Vin*	+0.5 to V_{EE}	V
Output Current	*Iout*	−30	mA
Storage Temperature	*Tstg*	−65 to +150	°C
Storage Temperature	*Tstg* (Bias) *	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS ($V_{EE}=-5.2V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min.(B)	typ.	max.(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	− 840	mV
			+25°C	− 960	—	− 810	
			+75°C	− 900	—	− 720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	− 980	—	—	
			+75°C	− 920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	− 840	mV
			+25°C	−1105	—	− 810	
			+75°C	−1045	—	− 720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	$0 \leqq Ta < 25°C$	− 150	−100	—	mA
			$Ta \geqq 25°C$	− 125	− 90	—	

●AC CHARACTERISTICS ($V_{EE}=-5.2V \pm 5\%$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			HM2110-2			Unit
			min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	
Chip Select Access Time	t_{ACS}		—	7	10	—	7	10	—	7	10	ns
Chip Select Recovery Time	t_{RCS}		—	7	10	—	7	10	—	7	10	ns
Address Access Time	t_{AA}		—	20	35	—	15	25	—	15	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			HM2110-2			Unit
			min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	
Write Pulse Width	t_W	$t_{WSA}=8ns$	25	—	—	25	—	—	25	—	—	ns
Data Setup Time	t_{WSD}		5	—	—	5	—	—	5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	5	—	—	5	—	—	ns
Address Setup Time	t_{WSA}	$t_W=25ns$	8	—	—	8	—	—	8	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	—	—	5	—	—	5	—	—	ns
Chip Select Hold Time	t_{WHCS}		5	—	—	5	—	—	5	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	10	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	—	—	10	—	—	10	ns

3. RISE/FALL TIME

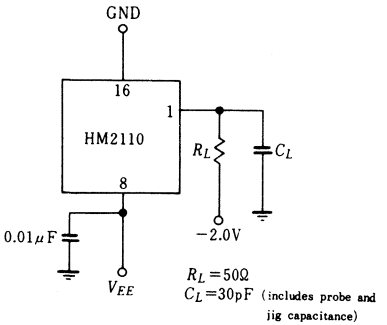
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Output Rise Time	t_r		—	5	—	ns
Output Fall Time	t_f		—	5	—	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}		—	4	5	pF
Output Capacitance	C_{out}		—	7	8	pF

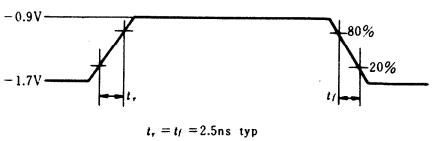
■TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION



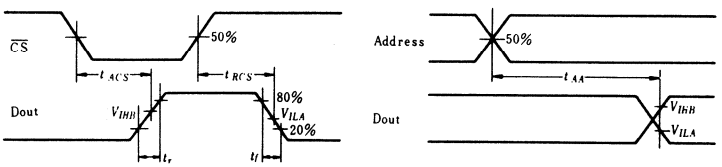
$R_L = 50\Omega$
$C_L = 30pF$ (includes probe and jig capacitance)

2. INPUT PULSE

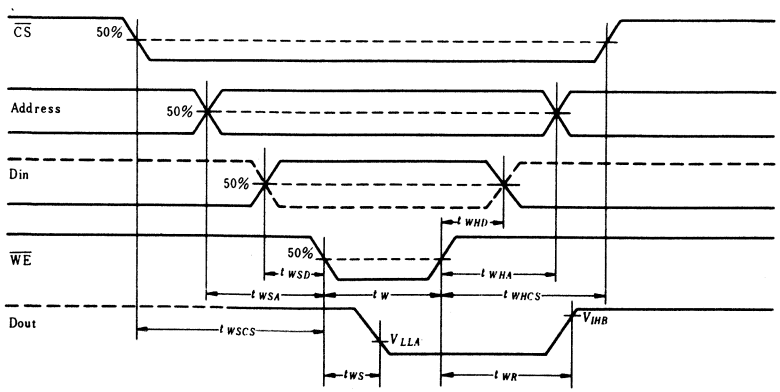


$t_r = t_f = 2.5ns$ typ

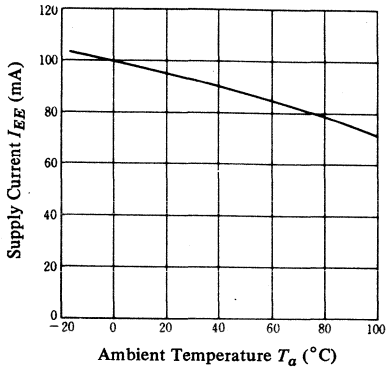
3. READ MODE



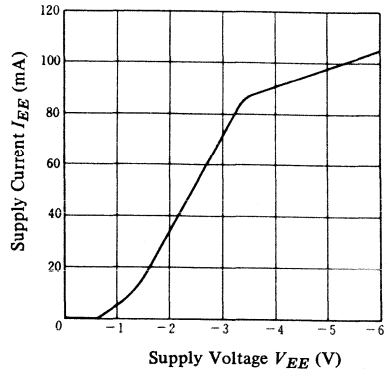
4. WRITE MODE



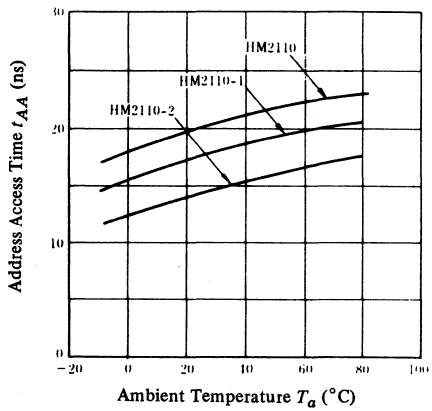
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



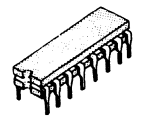
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



HM2112, HM2112-1

1024-word×1-bit Fully Decoded Random Access Memory

The HM2112 is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.



(DG-16A)

■ FEATURES

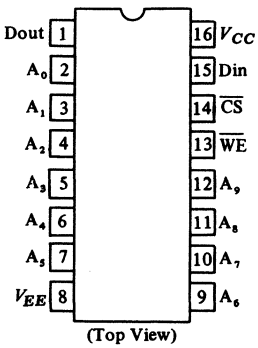
- Level ..... 10k ECL Compatible
- Construction ..... 1024-word by 1-bit
- Address Access Time ..... HM 2112 10ns (max.)
  HM2112-1 8ns (max.)
- Chip Select Access Time ..... 6ns (max.)
- Power Consumption ..... 0.8mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

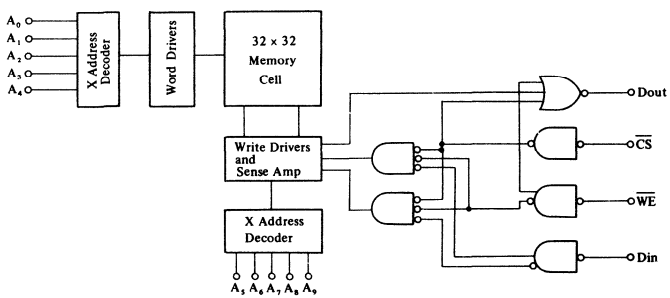
X : Irrelevant * : Read out noniverted

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2112	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS (V_{EE}=−5.2V, R_L=50Ω to −2.0V, Ta=0 to +75℃, air flow exceeding 2m/sec)

• DC CHARACTERISTICS

Item	Symbol	Test Condition		B	typ.	A	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0℃	−1000	—	−840	mV
			+25℃	−960	—	−810	
			+75℃	−900	—	−720	
	V_{OL}		0℃	−1870	—	−1665	
			+25℃	−1850	—	−1650	
			+75℃	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0℃	−1020	—	—	mV
			+25℃	−980	—	—	
			+75℃	−920	—	—	
	V_{OLC}		0℃	—	—	−1645	
			+25℃	—	—	−1630	
			+75℃	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0℃	−1145	—	−840	mV
			+25℃	−1105	—	−810	
			+75℃	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0℃	−1870	—	−1490	
			+25℃	−1850	—	−1475	
			+75℃	−1830	—	−1450	
Input Current	I_{IL}	$V_{IN}=V_{IHA}$	0 to +75℃	—	—	220	μA
	I_{IL}	$\overline{CS}$	0 to +75℃	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	Ta=0℃	− 230	− 180	—	mA
			Ta=75℃	—	− 150	—	

• AC CHARACTERISTICS (V_{EE}=−5.2V ±5%, Ta=0 to +75℃, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min.	typ.	max.	min.	typ.	max.	
Chip Select Access Time	t_{ACS}		1	3	6	1	3	6	ns
Chip Select Recovery Time	t_{RCS}		1	3	6	1	3	6	ns
Address Access Time	t_{AA}		3	6.5	8	3	7.5	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min.	typ.	max.	min.	typ.	max.	
Write Pulse Width	t_W	t_{WSA} = 3ns	7	2	–	7	2	–	ns
Data Setup Time	t_{WSD}		1	0	–	1	0	–	ns
Data Hold Time	t_{WHD}		1	0	–	1	0	–	ns
Address Setup Time	t_{WSA}	t_W = 7ns	3	0	–	3	0	–	ns
Address Hold Time	t_{WHA}		2	0	–	2	0	–	ns
Chip Select Setup Time	t_{WSCS}		1	0	–	1	0	–	ns
Chip Select Hold Time	t_{WHCS}		1	0	–	1	0	–	ns
Write Disable Time	t_{WS}		5	3	1	5	3	1	ns
Write Recovery Time	t_{WR}		1	3	5	1	3	5	ns

3. RISE/FALL TIME

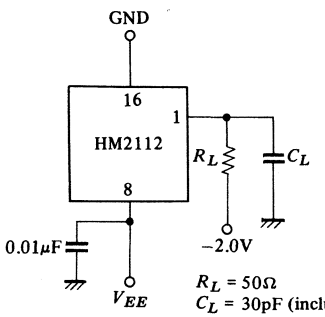
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Output Rise Time	t_r		0.8	1.5	2.5	ns
Output Fall Time	t_f		0.8	1.5	2.5	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}		1	3	5	pF
Output Capacitance	C_{out}		3	5	8	pF

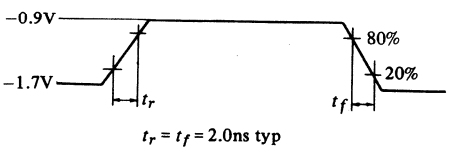
■ TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION



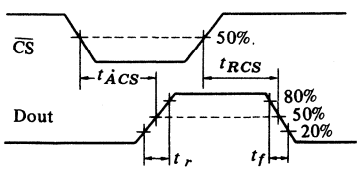
R_L = 50Ω
C_L = 30pF (includes probe and jig capacitance)

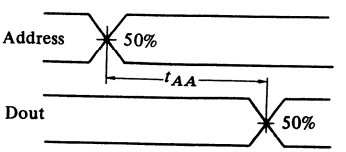
2. INPUT PULSE



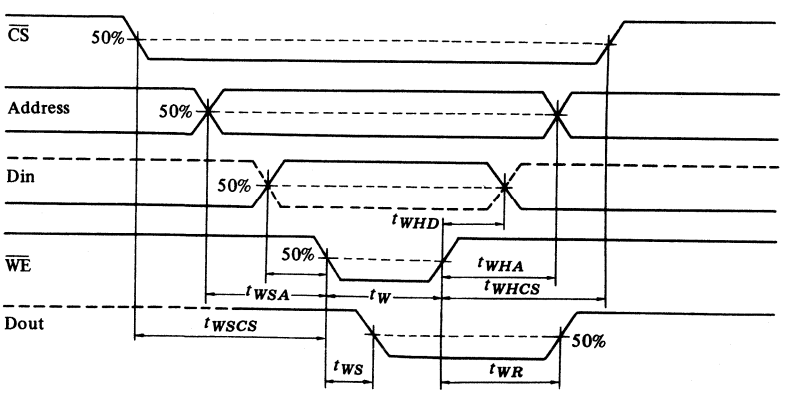
$t_r = t_f$ = 2.0ns typ

3. READ MODE

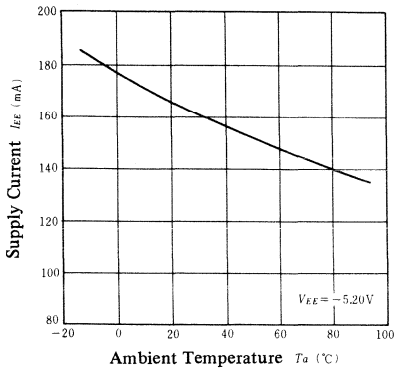




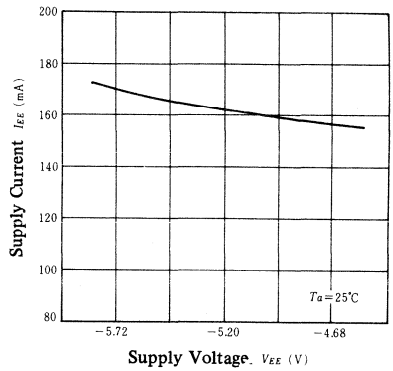
4. WRITE MODE



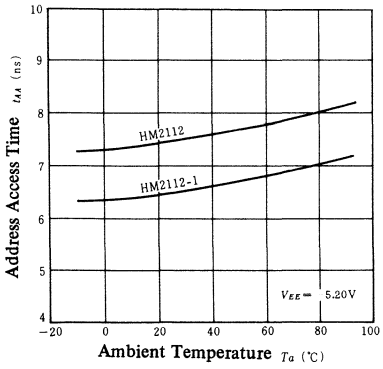
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



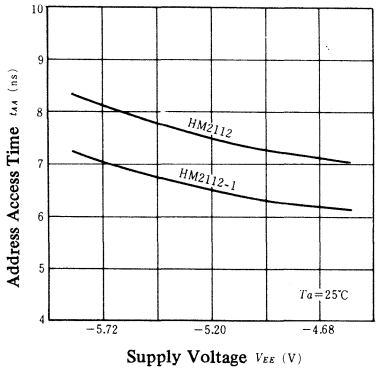
SUPPLY CURRENT vs. SUPPLY VOLTAGE



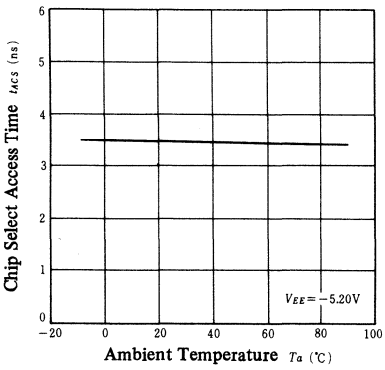
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



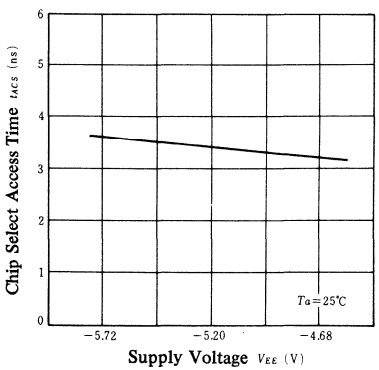
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



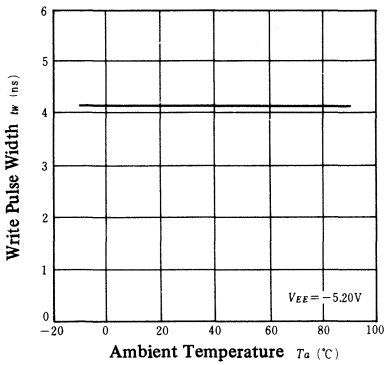
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



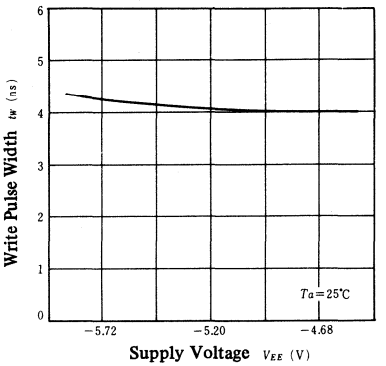
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



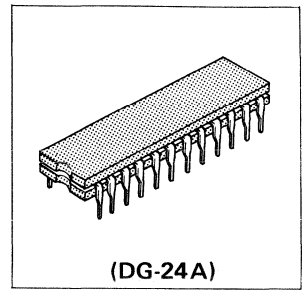
256-word × 4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10422 is encapsulated in cerdip-24pin package, or 24pin flat package, compatible with Fairchild's F10422.

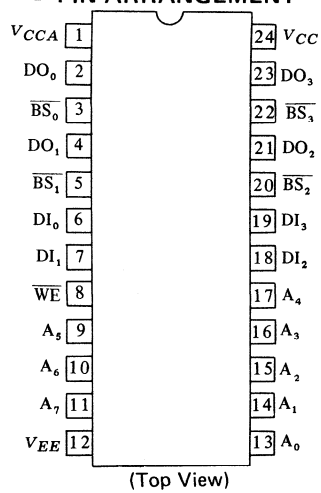


(DG-24A)

■ FEATURES

- 256-word x 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: 10ns (max)
- Write pulse width: 6ns(min)
- Power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



(Top View)

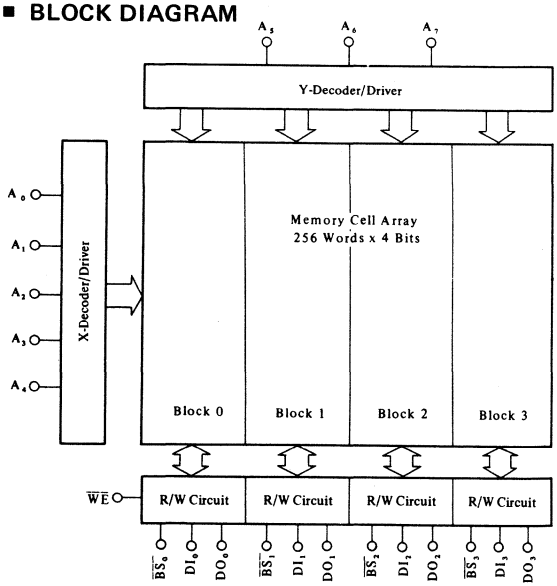
■ TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes: × ; irrelevant

* ; Read Out Noninvert

■ BLOCK DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V, R_L = 50 Ω to −2.0 V, T_a = 0 to +75°C, air flow exceeding 2 m/sec)

•DC CHARACTERISTICS

Item	Symbol	Test Condition		B	typ.	A	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	–	−840	mV
			+25°C	−960	–	−810	
			+75°C	−900	–	−720	
	V_{OL}		0°C	−1870	–	−1665	
			+25°C	−1850	–	−1650	
			+75°C	−1830	–	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	–	–	mV
			+25°C	−980	–	–	
			+75°C	−920	–	–	
	V_{OLC}		0°C	–	–	−1645	
			+25°C	–	–	−1630	
			+75°C	–	–	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	–	−840	mV
			+25°C	−1105	–	−810	
			+75°C	−1045	–	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	–	−1490	
			+25°C	−1850	–	−1475	
			+75°C	−1830	–	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	–	–	220	μA
	I_{IL}	$\overline{BS}$	0 to +75°C	0.5	–	170	
		Other		−50	–	–	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	T_a = 0°C	−200	−160	–	mA
			T_a = 75°C	–	−145	–	

• AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Block Select Access Time	t_{ABS}		–	–	5	ns
Block Select Recovery Time	t_{RBS}		–	–	5	ns
Address Access Time	t_{AA}		–	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Write Pulse Width	t_W	t_{WSA} = 2 ns	6	4.5	–	ns
Data Setup Time	t_{WSD}		–	0	–	ns
Data Hold Time	t_{WHD}		–	0	–	ns
Address Setup Time	t_{WSA}	t_W = 6 ns	2	0	–	ns
Address Hold Time	t_{WHA}		–	0	–	ns
Block Select Setup Time	t_{WSBS}		–	0	–	ns
Block Select Hold Time	t_{WHBS}		–	0	–	ns
Write Disable Time	t_{WS}		–	4	–	ns
Write Recovery Time	t_{WR}		–	4.5	–	ns

3. RISE/FALL TIME

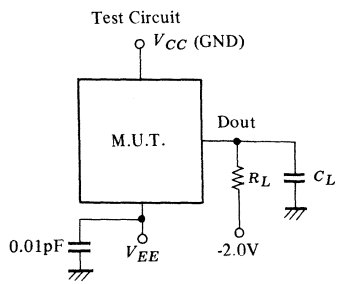
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Output Rise Time	t_r		–	2	–	ns
Output Fall Time	t_f		–	2	–	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}		–	4	–	pF
Output Capacitance	C_{out}		–	7	–	pF

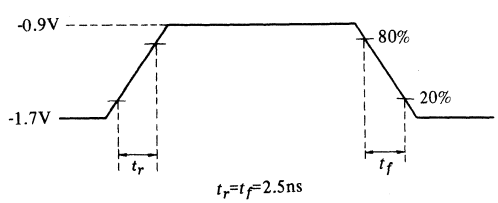
■ TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION



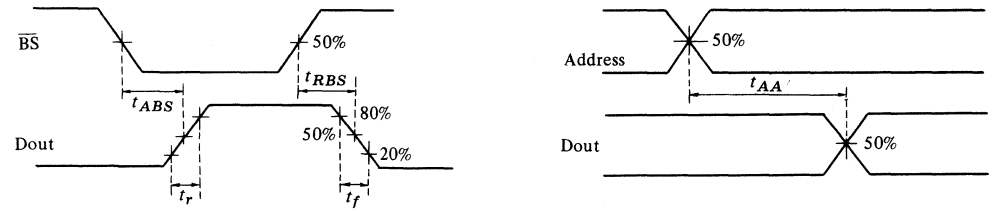
R_L=50Ω
C_L=30pF (includes probe and jig capacitance)

2. INPUT PULSE

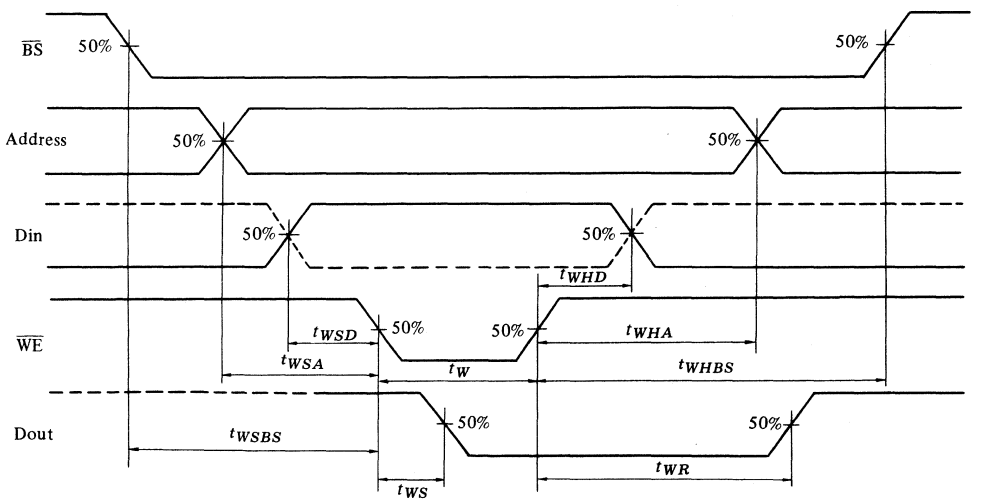


t_r=t_f=2.5ns

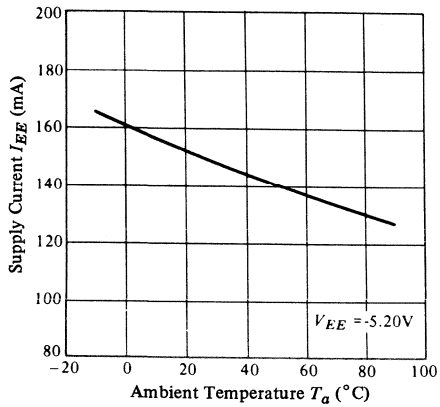
3. READ MODE



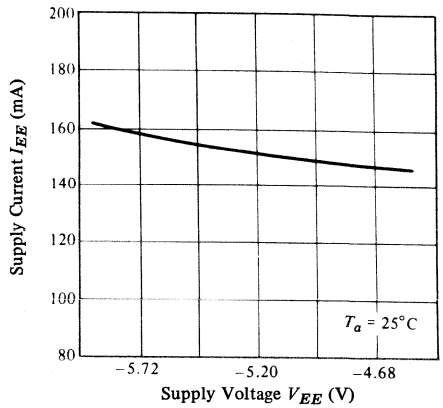
4. WRITE MODE



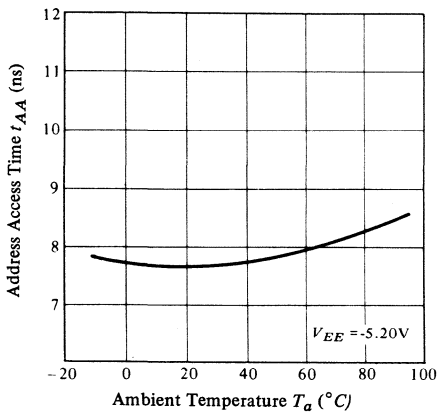
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



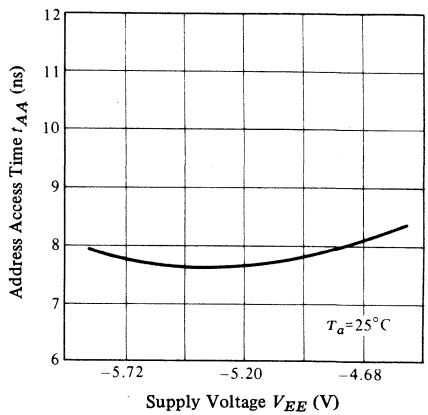
SUPPLY CURRENT VS. SUPPLY VOLTAGE



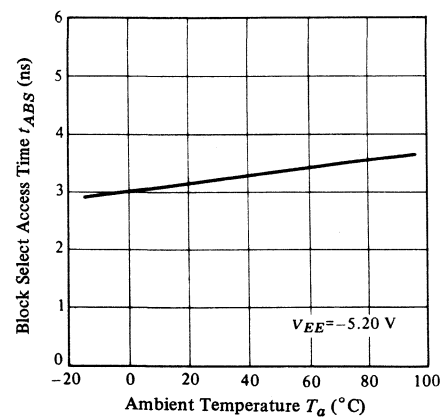
ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



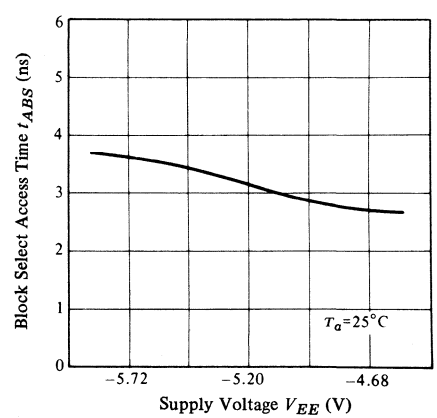
ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE



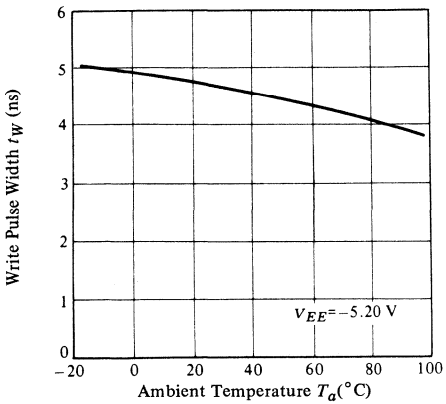
BLOCK SELECT ACCESS TIME VS. AMBIENT TEMPERATURE



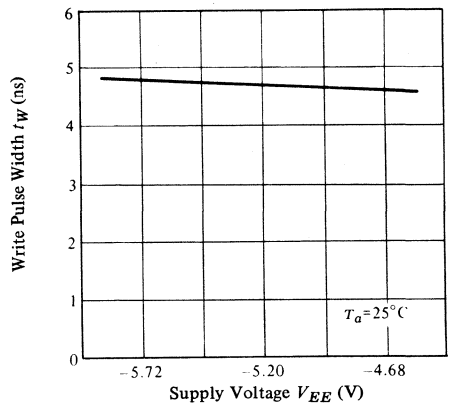
BLOCK SELECT ACCESS TIME VS. SUPPLY VOLTAGE



WRITE PULSE WIDTH VS. AMBIENT TEMPERATURE



WRITE PULSE WIDTH VS. SUPPLY VOLTAGE



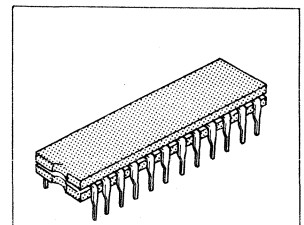
256-word × 4-bit Fully Decoded Random Access Memory

The HM100422 is ECL 100K compatible, 256-word x 4-bit, read/write, random access memory developed for high speed system such as scratch pads and control/buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100422 is encapsulated in cerdip-24pin package, or 24pin flat package compatible with Fairchild's F100422.



(DG-24A)

■ FEATURES

- 256-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10ns (max.)
- Minimum write pulse width: 6ns (min.)
- Low power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

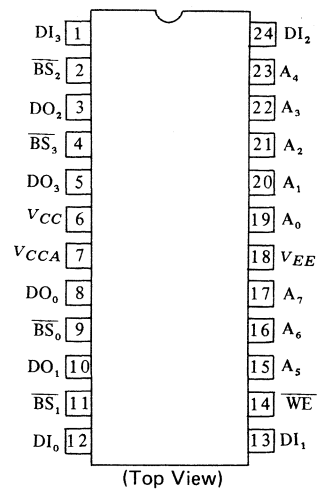
■ TRUTH TABLE

Item			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes: × ; irrelevant

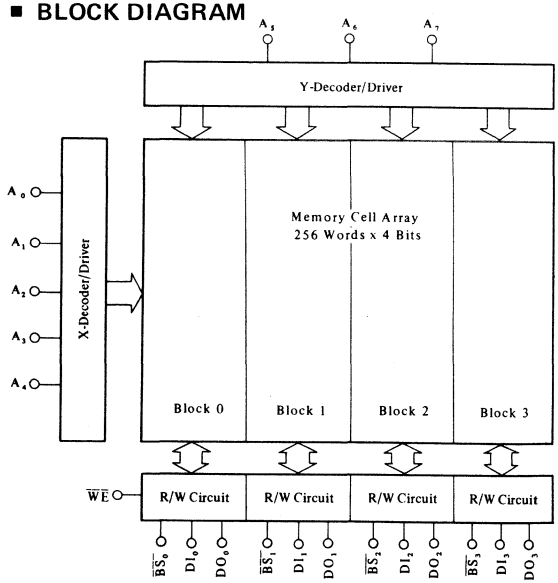
* ; Read Out Noninvert

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE}=-4.5V, R_L=50Ω to-2.0V, T_a=0 to + 85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		B	typ.	A	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILB}		−1035	–	–	mV
	V_{OLC}			–	–	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	–	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	–	−1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		–	–	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{BS}$	0.5	–	170	μA
			Others	−50	–	–	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	–	mA

● AC CHARACTERISTICS (V_{EE}=-4.5V±5%, T_a=0 to + 85°C, air flow exceeding 2m/sec).

1. READ MODE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Block Select Access Time	t_{ABS}		–	–	5	ns
Block Select Recovery Time	t_{RBS}		–	–	5	ns
Address Access Time	t_{AA}		–	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Write Pulse Width	t_W	t_{WSA} = 2 ns	6	4.5	–	ns
Data Setup Time	t_{WSD}		–	0	–	ns
Data Hold Time	t_{WHD}		–	0	–	ns
Address Setup Time	t_{WSA}	t_W = 6 ns	2	0	–	ns
Address Hold Time	t_{WHA}		–	0	–	ns
Block Select Setup Time	t_{WSBS}		–	0	–	ns
Block Select Hold Time	t_{WHBS}		–	0	–	ns
Write Disable Time	t_{WS}		–	4	–	ns
Write Recovery Time	t_{WR}		–	4.5	–	ns

3. RISE/FALL TIME

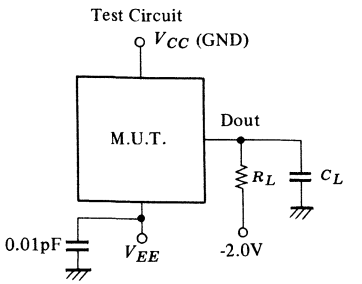
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Output Rise Time	t_r		–	2	–	ns
Output Fall Time	t_f		–	2	–	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}		–	4	–	pF
Output Capacitance	C_{out}		–	7	–	pF

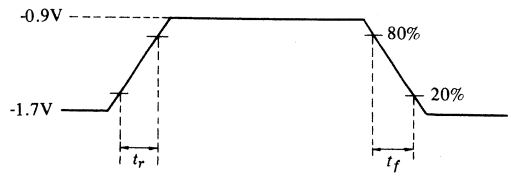
■ TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION



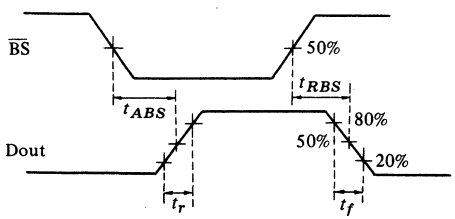
R_L=50Ω
C_L=30pF (includes probe and jig capacitance)

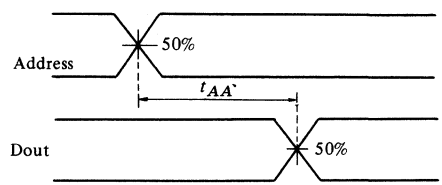
2. INPUT PULSE



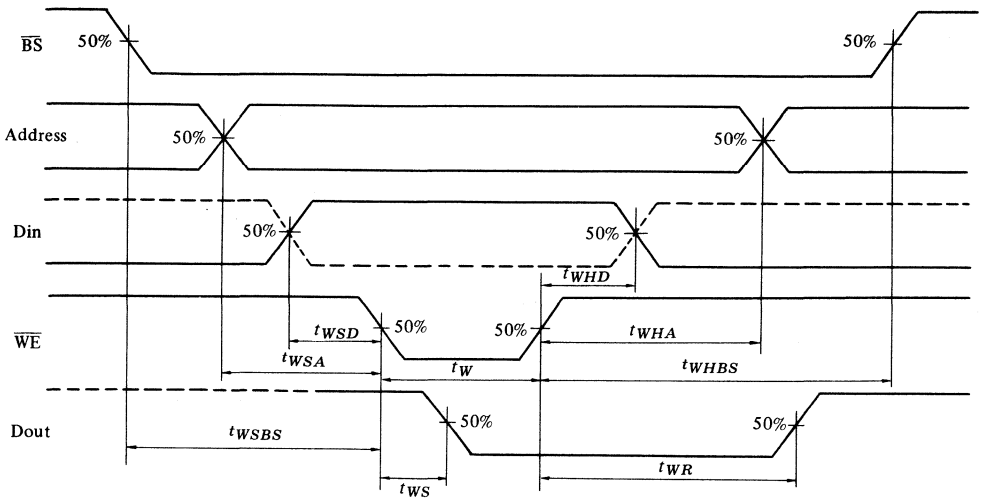
t_r=t_f=2.5ns

3. READ MODE





4. WRITE MODE

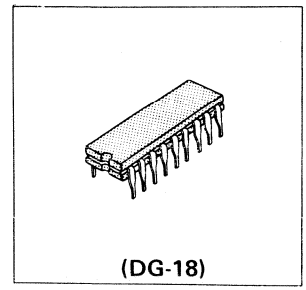

$\overline{BS}$
50%
50%
Address
50%
50%
Din
50%
50%
t_{WHD}
$\overline{WE}$
t_{WSD}
50%
50%
t_{WHA}
t_{WSA}
t_W
t_{WHBS}
Dout
t_{WSBS}
50%
50%
t_{WR}
t_{WS}

4096-word × 1-bit Fully Decoded Random Access Memory

The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10470 is encapsulated in cerdip-18pin package, compatible with Fairchild's F10470.

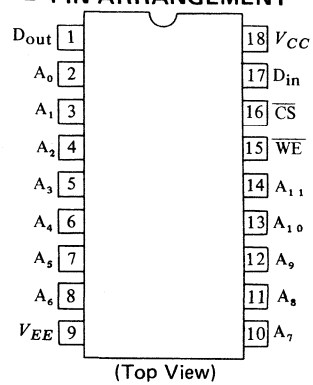


(DG-18)

■ FEATURES

- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10470 25 ns (max)
  HM10470-1 15 ns (max)
- Write pulse width: HM10470 20 ns (min)
  HM10470-1 15 ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



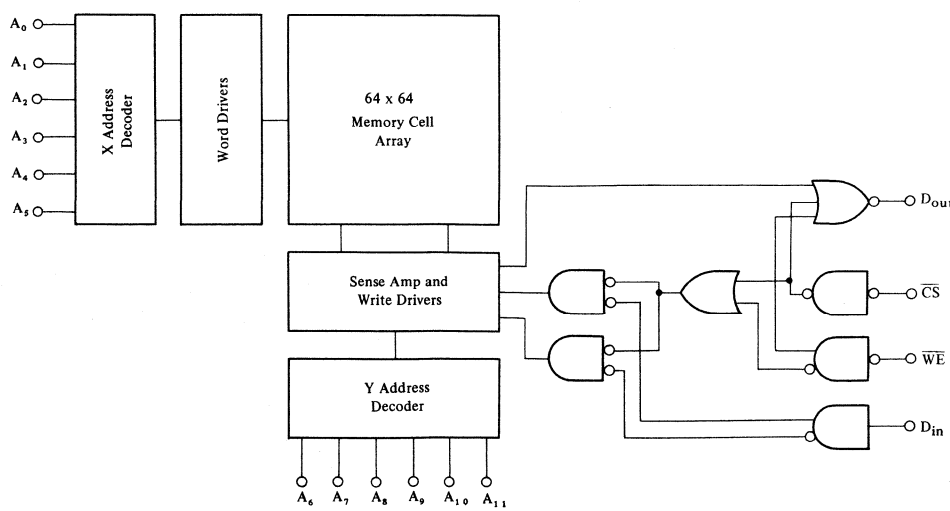
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	x	x	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	x	Dout*	Read

Notes) x; irrelevant
*; Read Out Noninvert

■ BLOCK DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

■ TEST CIRCUIT AND WAVEFORMS

● DC CHARACTERISTICS (V_{EE}=-5.2V, R_L=50 Ω to-2.0V, T_a=0 to + 75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		B	typ.	A	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	–	−840	mV
			+25°C	−960	–	−810	
			+75°C	−900	–	−720	
	V_{OL}		0°C	−1870	–	−1665	
			+25°C	−1850	–	−1650	
			+75°C	−1830	–	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	–	–	mV
			+25°C	−980	–	–	
			+75°C	−920	–	–	
	V_{OLC}		0°C	–	–	−1645	
			+25°C	–	–	−1630	
			+75°C	–	–	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	–	−840	mV
			+25°C	−1105	–	−810	
			+75°C	−1045	–	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	–	−1490	
			+25°C	−1850	–	−1475	
			+75°C	−1830	–	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	–	–	220	μA
	I_{IL}	$\overline{BS}$	0 to +75°C	0.5	–	170	
		Other		−50	–	–	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 9	T_a = 0°C	−200*	−160*		mA
				−230**	−180**	–	
			T_a = 75°C	–	−145	–	

*HM10470 **HM10470-1

● AC CHARACTERISTICS (V_{EE}=-5.2V±5%, T_a=0 to + 75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	HM10470			HM10470-1			Unit
			min.	typ.	max.	min.	typ.	max.	
Chip Select Access Time	t_{ACS}		–	–	10	–	–	8	ns
Chip Select Recovery Time	t_{RCS}		–	–	10	–	–	8	ns
Address Access Time	t_{AA}		–	–	25	–	–	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10470			HM10470-1			Unit
			min.	typ.	max.	min.	typ.	max.	
Write Pulse Width	t_W	t_{WSA} = 3 ns	20	–	–	15	–	–	ns
Data Setup Time	t_{WSD}		2	–	–	2	–	–	ns
Data Hold Time	t_{WHD}		2	–	–	2	–	–	ns
Address Setup Time	t_{WSA}	t_W = 20 ns	3	–	–	3	–	–	ns
Address Hold Time	t_{WHA}		2	–	–	2	–	–	ns
Chip Select Setup Time	t_{WSCS}		2	–	–	2	–	–	ns
Chip Select Hold Time	t_{WHCS}		2	–	–	2	–	–	ns
Write Disable Time	t_{WS}		–	–	10	–	–	8	ns
Write Recovery Time	t_{WR}		–	–	10	–	–	8	ns

3. RISE/FALL TIME

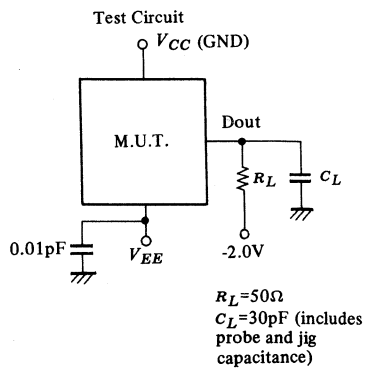
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Output Rise Time	t_r		–	2	–	ns
Output Fall Time	t_f		–	2	–	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}		–	3	–	pF
Output Capacitance	C_{out}		–	5	–	pF

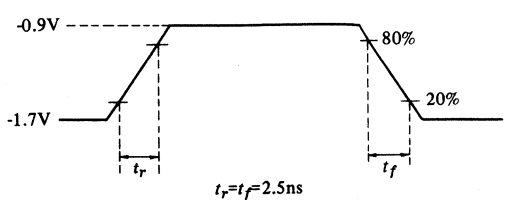
■ TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION



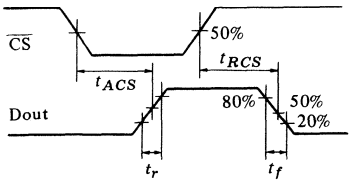
R_L=50Ω
C_L=30pF (includes probe and jig capacitance)

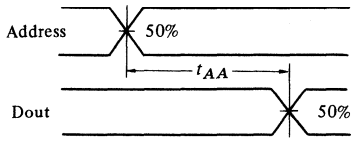
2. INPUT PULSE



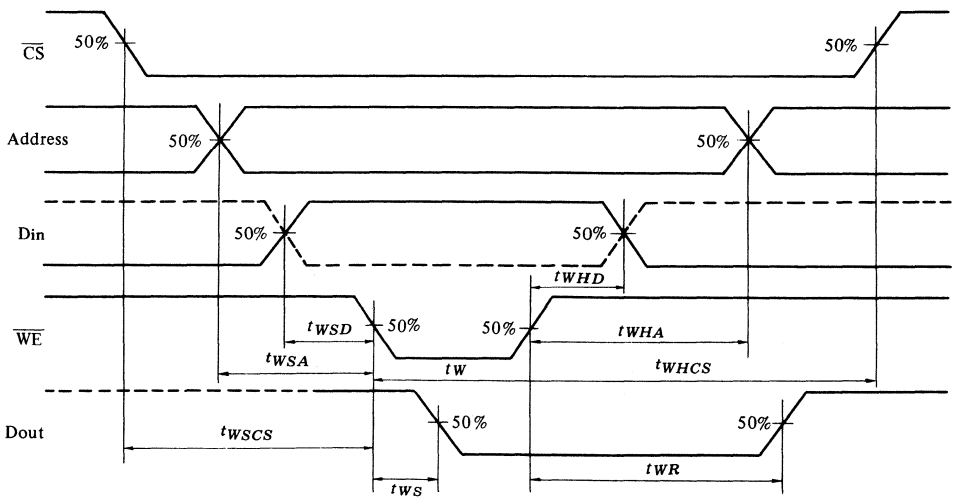
t_r=t_f=2.5ns

3. READ MODE

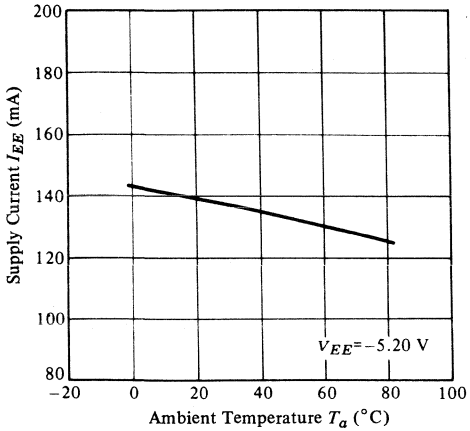




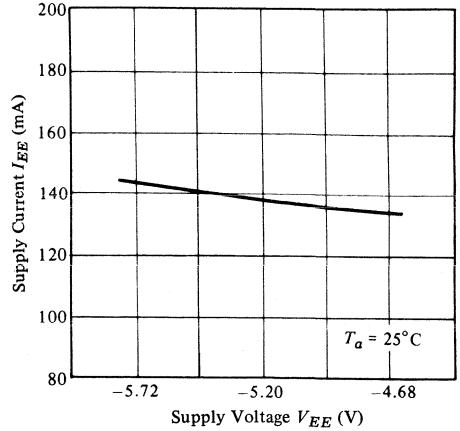
4. WRITE MODE



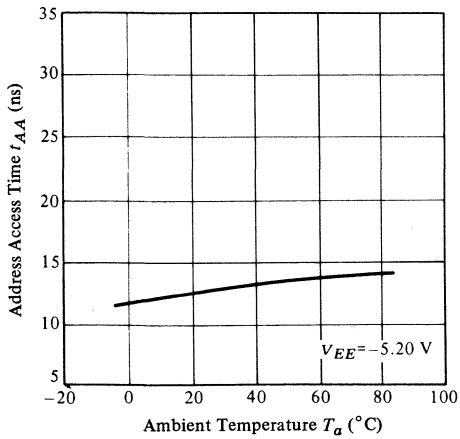
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



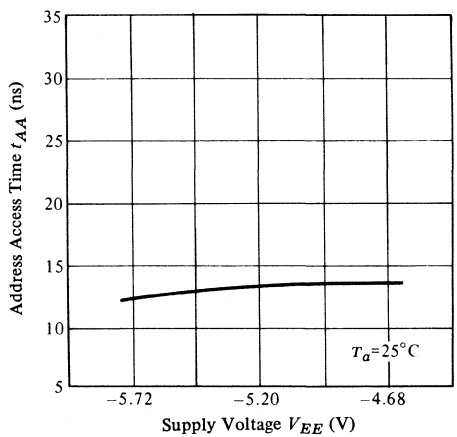
SUPPLY CURRENT VS. SUPPLY VOLTAGE



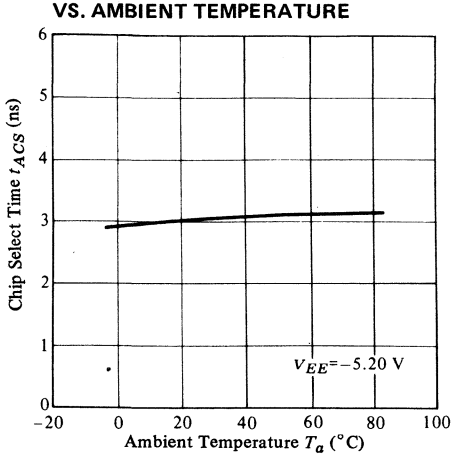
ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



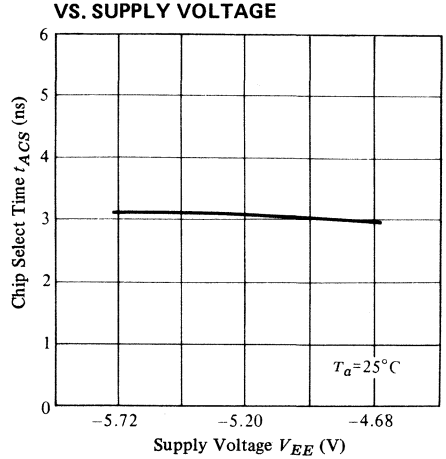
ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE



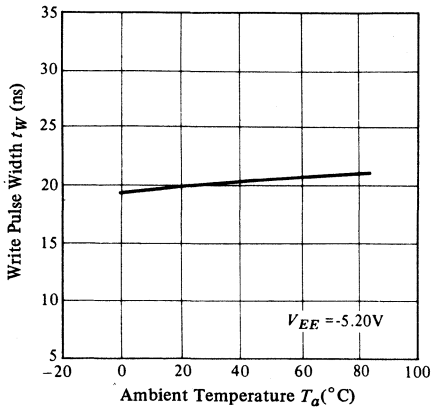
CHIP SELECT ACCESS TIME VS. AMBIENT TEMPERATURE



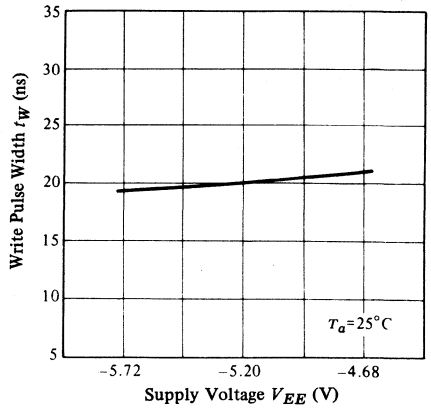
CHIP SELECT ACCESS TIME VS. SUPPLY VOLTAGE



WRITE PULSE WIDTH VS. AMBIENT TEMPERATURE



WRITE PULSE WIDTH VS. SUPPLY VOLTAGE

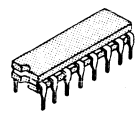


HM2504, HM2504-1

256-word × 1-bit Fully Decoded Random Access Memory

The HM2504 Series item is a TTL compatible, 256-word x 1-bit, read/write random access memory developed for application to buffer memories, control memories, high-speed main memories, etc. This is a fully decoded, read/write random access memory perfectly compatible with the standard DTL and TTL logic family, designed as an open collector output type for simplicity of expansion.

- Level ..... TTL compatible
- Construction ..... 256-word x 1 bit
- Read access time ..... HM2504: 55ns (max.)
  HM2504-1: 45ns (max.)
- Chip select access time ..... 30ns (max.)
- Power consumption ..... 1.8mW/bit (typ)
- Output ..... Open collector



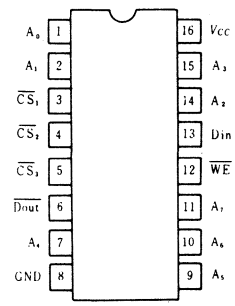
(DG-16)

■TRUTH TABLE

Inputs			Output Open Collector	Mode
$\overline{CS}$	$\overline{WE}$	Din		
any one H	×	×	H	Not Selected
all L	L	L	H	Write "0"
all L	L	H	H	Write "1"
all L	H	×	$\overline{Dout}$*	Read

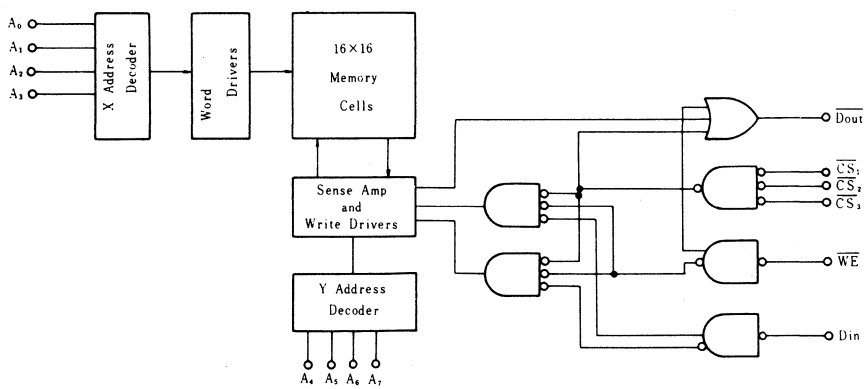
× : Don't care
* : Read out inverted

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2504, HM2504-1	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	Vin	−0.5 to +5.5	V
Input Current	Iin	−12 to +5.0	mA
Output Voltage (Output High)	$Vout$	−0.5 to +5.5	V
Output Voltage (DC Output Low)	$Iout$	+20	mA
Storage Temperature	$Tstg$	−65 to +150	°C
Storage Temperature	$Tstg$(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{CC}=5.0V±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		HM2504 Series min.	HM2504 Series typ.	HM2504 Series max.	Unit
Output Voltage	V_{OL}	V_{CC}=4.75V, I_{OL}=16mA		—	0.3	0.45	V
Input Voltage	V_{IH}	Guaranteed Input Voltage High		2.0	1.6	—	V
	V_{IL}	Guaranteed Input Voltage Low		—	1.5	0.85	V
Input Current	I_{IH}	V_{CC}=5.25V, Vin=4.5V		—	0	20	μA
	I_{IL}	V_{CC}=5.25V, Vin=0		—	−530	−800	μA
Output Leakage Current	I_{CEX}	V_{CC}=5.25V, $Vout$=4.5V		—	0	50	μA
Input Clamp Voltage	V_I	V_{CC}=5.25V, Iin=−10mA		—	−1.0	−1.5	V
Supply Current	I_{CC}	V_{CC}=5.25V, All input GND	0< Ta<25°C	—	—	135	mA
			Ta≧25°C	—	—	130	mA

●AC CHARACTERISTICS (V_{CC}=5.0V±5%, Ta=0 to +75°C, air flow exceeding 2m/s, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2504 min.	HM2504 typ.	HM2504 max.	HM2504-1 min.	HM2504-1 typ.	HM2504-1 max.	Unit
Chip Select Access Time	t_{ACS}		—	12	30	—	12	30	ns
Chip Select Recovery Time	t_{RCS}		—	18	25	—	18	25	ns
Address Access Time	t_{AA}		—	35	55	—	30	45	ns

2. WRITE MODE

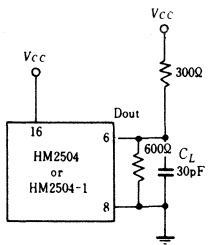
Item	Symbol	Test Condition	HM2504 min.	HM2504 typ.	HM2504 max.	HM2504-1 min.	HM2504-1 typ.	HM2504-1 max.	Unit
Write Pulse Width	t_W	t_{WSA}=0ns	30	8	—	30	8	—	ns
Data Setup Time	t_{WSD}		0	0	—	0	0	—	ns
Data Hold Time	t_{WHD}		5	0	—	5	0	—	ns
Address Setup Time	t_{WSA}	t_W=30ns	0	0	—	0	0	—	ns
Address Hold Time	t_{WHA}		5	0	—	5	0	—	ns
Chip Select Setup Time	t_{WSCS}		0	0	—	0	0	—	ns
Chip Select Hold Time	t_{WHCS}		5	0	—	5	0	—	ns
Write Disable Time	t_{WS}		—	14	35	—	14	35	ns
Write Recovery Time	t_{WR}		—	12	40	—	12	40	ns

3. CAPACITANCE

Item	Symbol	Test Condition	HM2504			HM2504-1			Unit
			min.	typ.	max.	min.	typ.	max.	
Input Capacitance	*Cin*		—	3	5	—	3	5	pF
Output Capacitance	*Cout*		—	6	8	—	6	8	pF

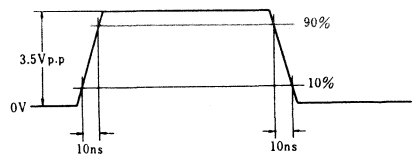
■TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION

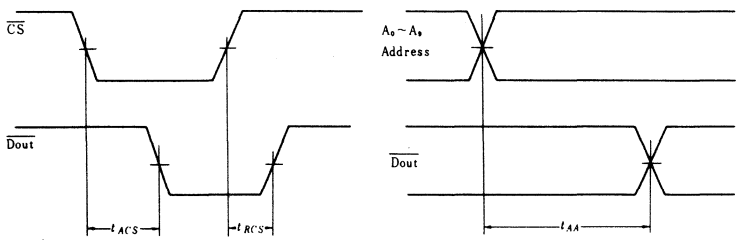


Note: C_L includes jig and stray capacitance

2. INPUT PULSES

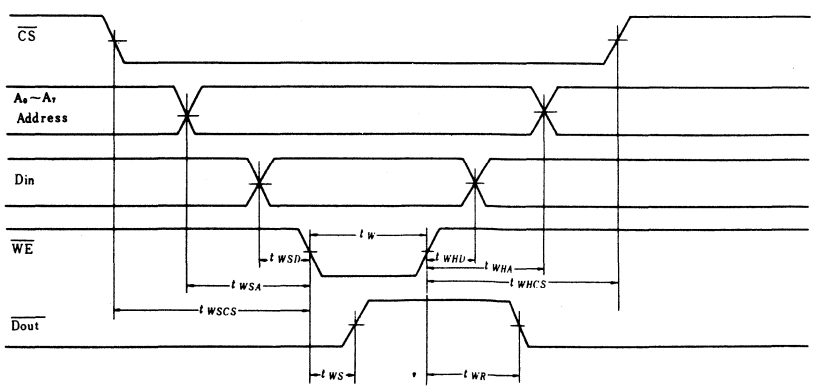


3. READ MODE



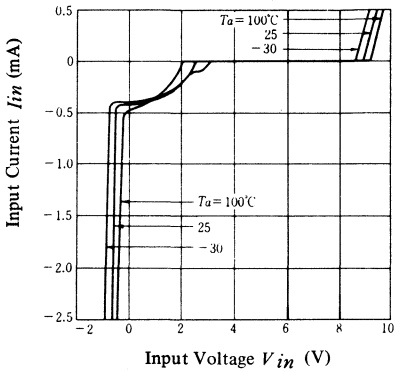
(All time measurements refer to 1.5V)

4. WRITE MODE

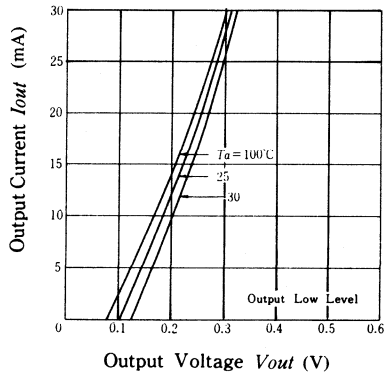


(All time measurements refer to 1.5V)

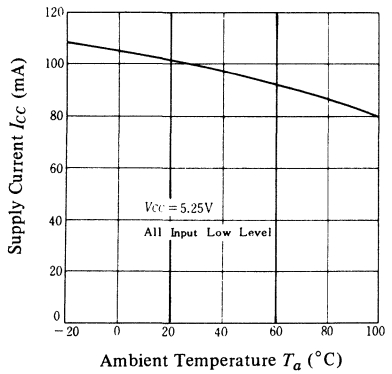
INPUT CHARACTERISTICS



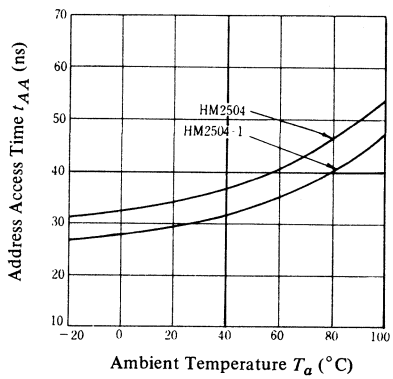
OUTPUT CHARACTERISTICS



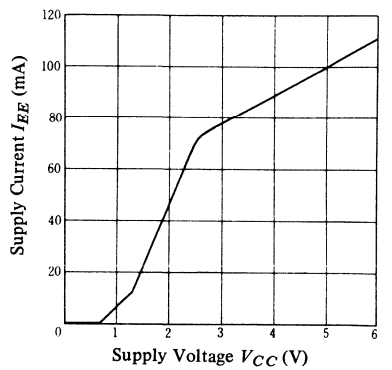
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

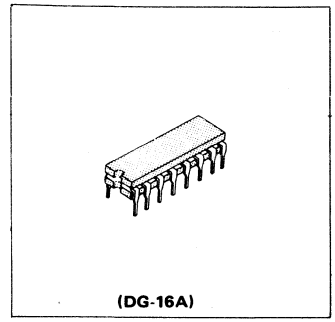


HM2510, HM2510-1, HM2510-2

1024-word × 1-bit Fully Decoded Random Access Memory

The HM 2510 Series item is a 1024-word x 1-bit read/write random access memory developed for application to buffer memories, control memories, high-speed main memories, etc. It is a fully decoded, read/write, random access memory perfectly compatible with standard DTL and TTL logic families, desigend as an open collector output type for simplicity of expansion.

- Level ..... TTL compatible
- Construction ..... 1024-word x 1 bit
- Read access time ..... HM2510: 70ns (max.)
  HM2510-1: 45ns (max.)
  HM2510-2: 35ns (max.)
- Chip select access time ..... HM2510: 40ns (max.)
  HM2510-1: 30ns (max.)
  HM2510-2: 25ns (max.)
- Power consumption 0.5mW/bit
- Output ..... Open collector



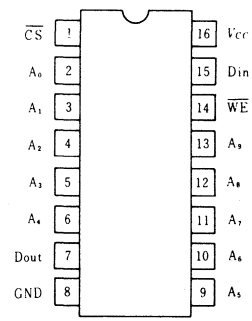
(DG-16A)

■TRUTH TABLE

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	×	Dout *	Read

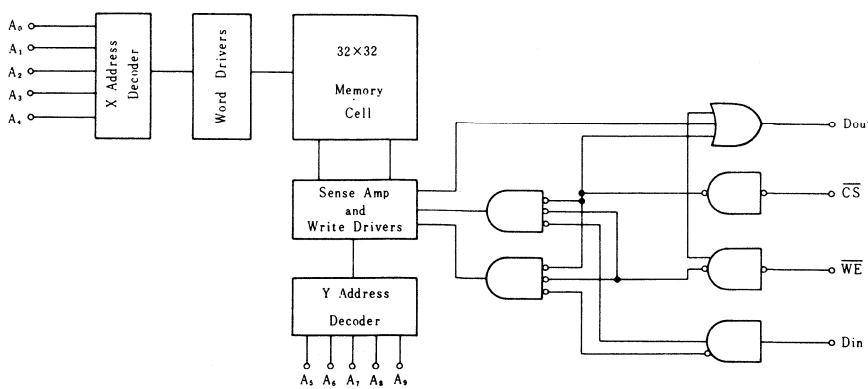
× : Don't care
* : Read out non-inverted

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2510 Series	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	Vin	−0.5 to +5.5	V
Input Current	Iin	−12 to +5.0	mA
Output Voltage (Output High)	$Vout$	−0.5 to +5.5	V
Output Voltage (DC Output Low)	$Iout$	+20	mA
Storage Temperature	$Tstg$	−65 to +150	°C
Storage Temperature	$Tstg$(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{CC}=5.0V±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		HM2510 Series			Unit
				min.	typ.	max.	
Output Voltage	V_{OL}	V_{CC}=4.75V, I_{OL}=16mA		—	0.3	0.45	V
Input Voltage	V_{IH}	Guaranteed Input Voltage High		2.1	1.6	—	V
	V_{IL}	Guaranteed Input Voltage Low		—	1.5	0.80	V
Input Current	I_{IH1}	V_{CC}=5.25V, Vin=4.5V		—	0	40	μA
	I_{IH2}	V_{CC}=5.25V, Vin=5.25V			0	1.0	mA
	I_{IL}	V_{CC}=5.25V, Vin=0.4V		—	−250	−400	μA
Output Leakage Current	I_{CEX}	V_{CC}=5.25V, $Vout$=4.5V		—	0	100	μA
Input Clamp Voltage	V_I	V_{CC}=5.25V, Iin=−10mA		—	−1.0	−1.5	V
Supply Current	I_{CC}	V_{CC}=5.25V	0< Ta<25°C	—	—	155	mA
		All input GND	Ta≧25°C	—	95	130	mA

● AC CHARACTERISTICS (V_{CC}=5.0V±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM2510			HM2510-1			HM2510-2			Unit
			min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	
Chip Select Access Time	t_{ACS}		—	15	40	—	—	30	—	15	25	ns
Chip Select Recovery Time	t_{RCS}		—	25	40	—	—	30	—	17	25	ns
Address Access Time	t_{AA}		—	40	70	—	35	45	—	25	35	ns

2. WRITE MODE

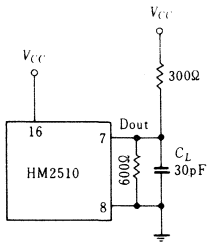
Item	Symbol	Test Condition	HM2510			HM2510-1			HM2510-2			Unit
			min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	
Write Pulse Width	t_W	t_{WSA}=min	50	10	—	35	10	—	25	10	—	ns
Data Setup Time	t_{WSD}		5	0	—	5	—	—	5	0	—	ns
Data Hold Time	t_{WHD}		5	0	—	5	—	—	5	0	—	ns
Address Setup Time	t_{WSA}	t_W=min	15	0	—	5	—	—	5	0	—	ns
Address Hold Time	t_{WHA}		5	0	—	5	—	—	5	0	—	ns
Chip Select Setup Time	t_{WSCS}		5	0	—	5	—	—	5	0	—	ns
Chip Select Hold Time	t_{WHCS}		5	0	—	5	—	—	5	0	—	ns
Write Disable Time	t_{WS}		—	20	40	—	20	35	—	15	25	ns
Write Recovery Time	t_{WR}		—	30	55	—	30	45	—	15	25	ns

3. CAPACITANCE

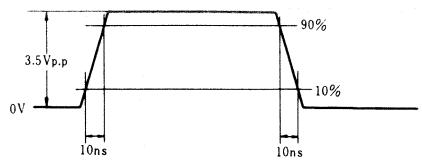
Item	Symbol	Test Condition	HM2510 Series			Unit
			min.	typ.	max.	
Input Capacitance	C_{in}		—	3	5	pF
Output Capacitance	C_{out}		—	6	8	pF

■TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION

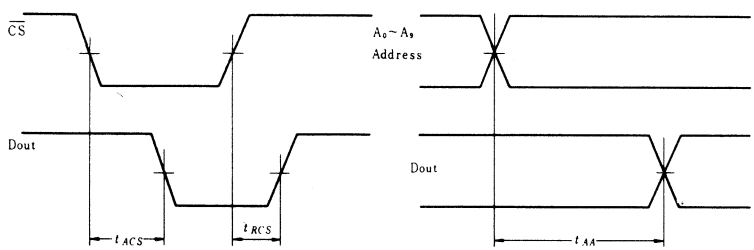


2. INPUT PULSE



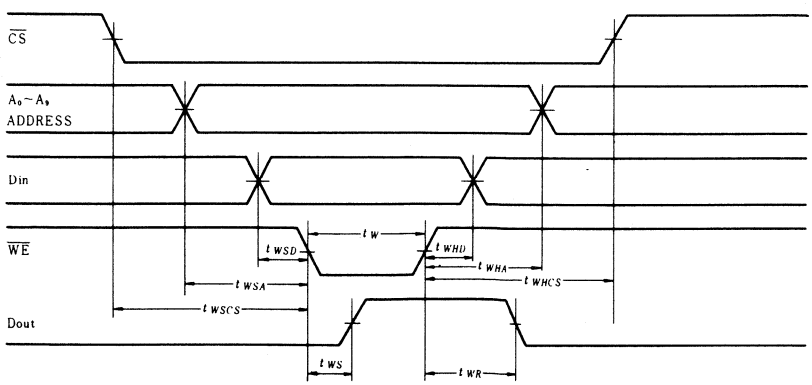
Note : C_L includes probe and stray capacitance

3. READ MODE



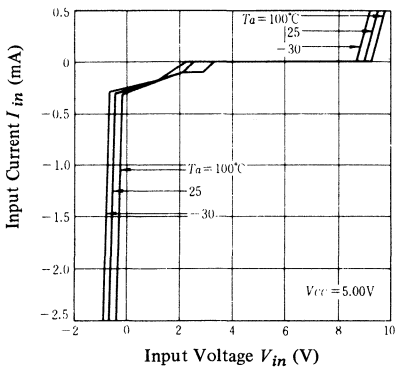
(All time measurements refer to 1.5V)

4. WRITE MODE

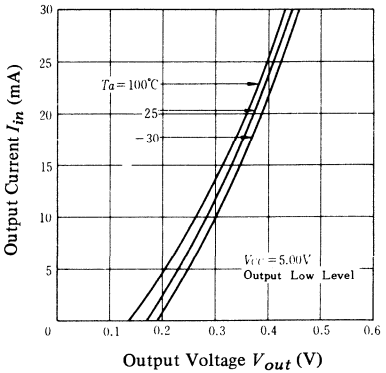


(All time measurements refer to 1.5V)

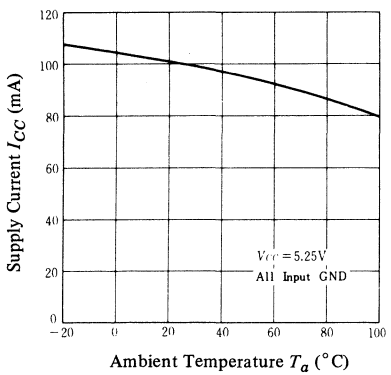
INPUT CHARACTERISTICS



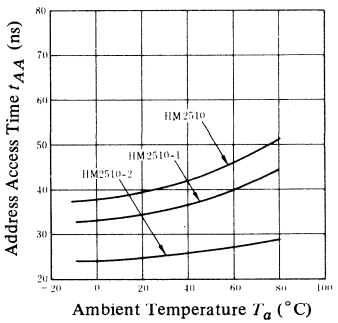
OUTPUT CHARACTERISTICS



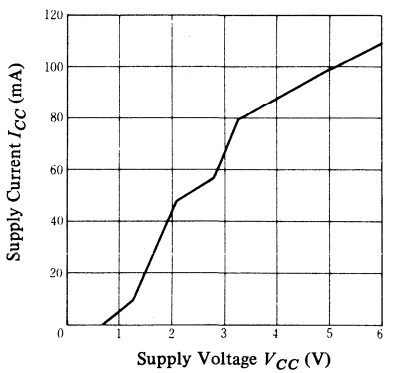
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

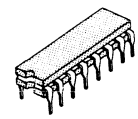


HM2511, HM2511-1

1024-word × 1-bit Fully Decoded Random Access Memory

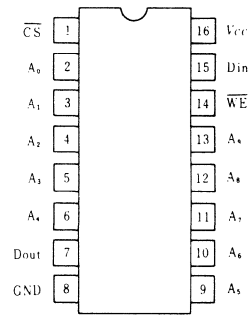
The HM2511 Series item is a 1024-word x 1-bit read/write random access memory with tri-state output developed for application to buffer memories, control memories, high-speed main memories, etc. It is a fully decoded, read/write, random access memory perfectly compatible with standard DTL and TTL logic families.

- Level ..... TTL compatible
- Construction ..... 1024-word x 1 bit
- Read access time ..... HM2511: 70ns (max)
  HM2511-1: 45ns (max)
- Chip select access time ..... HM2511: 40ns (max)
  HM2511-1: 30ns (max)
- Power consumption ..... 0.5 mW/bit
- Output ..... tri-state



(DG-16A)

■ PIN ARRANGEMENT



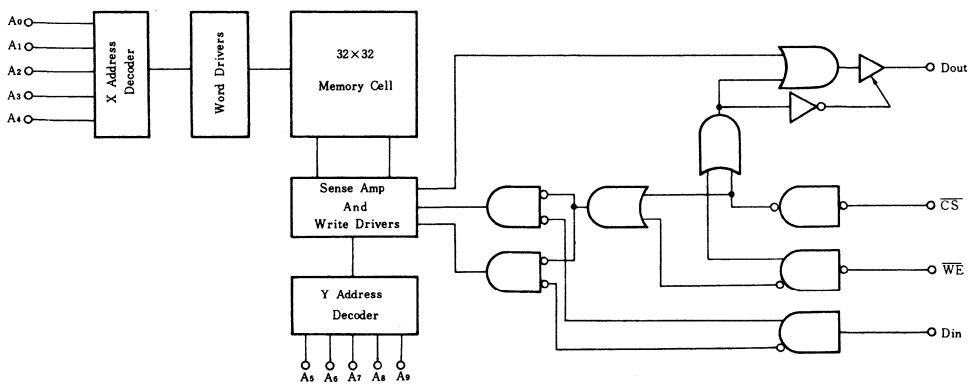
(Top View)

■ TRUTH TABLE

Input			Output Open Collector	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	High Z	Not Selected
L	L	L	High Z	Write "0"
L	L	H	High Z	Write "1"
L	H	×	Dout *	Read

× : Don't care
* : Read out noninverted

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2511 Series	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +5.5	V
Input Current	I_{in}	− 12 to +5.0	mA
Output Voltage (Output High)	V_{out}	−0.5 to +5.5	V
Output Voltage (DC Output Low)	I_{out}	+20	mA
Storage Temperature	T_{stg}	−65 to +150	℃
Storage Temperature	T_{stg} (Bias)*	−55 to +125	℃

* Under Bias

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC}=5.0V±5%, Ta=0 to +75℃, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		HM2511 Series min.	HM2511 Series typ.	HM2511 Series max.	Unit
Output Low Voltage	V_{OL}	V_{CC}=4.75V, I_{OL}=16mA		—	0.3	0.45	V
Input Voltage	V_{IH}	Guaranteed Input Voltage High		2.1	1.6	—	V
	V_{IL}	Guaranteed Input Voltage Low		—	1.5	0.8	V
Input Current	$I_{IH\ 1}$	V_{CC}=5.25V, V_{in}=4.5V		—	0	40	μA
	$I_{IH\ 2}$	V_{CC}=5.25V, V_{in}=5.25V		—	0	1.0	mA
	I_{IL}	V_{CC}=5.25V, V_{in}=0.4V		—	−250	−400	μA
Output Current (High Z)	$I_{OFF\ 1}$	V_{CC}=5.25V, V_{out}=2.4V		—	—	50	μA
	$I_{OFF\ 2}$	V_{CC}=5.25V, V_{out}=0.5V		—	—	−50	μA
Output Current Short Circuit to Ground	I_{OS}	V_{CC}=5.25V		—	—	−100	mA
Output High Voltage	V_{OH}	I_{OH}=−10.3mA, V_{CC}=5.0V±5%		2.4	—	—	V
Input Clamp Voltage	V_I	V_{CC}=5.25V, I_{in}=−10mA		—	−1.0	−1.5	V
Supply Current	I_{CC}	V_{CC}=5.25V	0≦Ta<25℃	—	—	155	mA
		All input GND	Ta≧25℃	—	95	130	mA

• AC CHARACTERISTICS (V_{CC}=5.0V±5%, Ta=0 to +75℃, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM2511 min.	HM2511 typ.	HM2511 max.	HM2511-1 min.	HM2511-1 typ.	HM2511-1 max.	Unit
Chip Select Access Time	t_{ACS}		—	15	40	—	—	30	ns
Chip Select to High Z	t_{ZRCS}		—	20	40	—	—	30	ns
Address Access Time	t_{AA}		—	40	70	—	35	45	ns

2. WRITE MODE

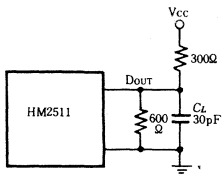
Item	Symbol	Test Condition	HM2511 min.	HM2511 typ.	HM2511 max.	HM2511-1 min.	HM2511-1 typ.	HM2511-1 max.	Unit
Write Pulse Width	t_W	t_{WSA}=min	50	25	—	35	10	—	ns
Data Setup Time	t_{WSD}		5	0	—	5	—	—	ns
Data Hold Time	t_{WHD}		5	0	—	5	—	—	ns
Address Setup Time	t_{WSA}	t_W=min	15	0	—	5	—	—	ns
Address Hold Time	t_{WHA}		5	0	—	5	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	0	—	5	—	—	ns
Chip Select Hold Time	t_{WHCS}		5	0	—	5	—	—	ns
Write Disable to High Z	t_{ZWS}		—	20	40	—	20	35	ns
Write Recovery Time	t_{WR}		—	42	55	—	30	45	ns

3. CAPACITANCE

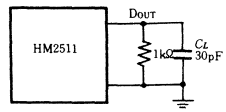
Item	Symbol	Test Condition	HM2511 Series			Unit
			min.	typ.	max.	
Input Capacitance	C_{in}		—	3	5	pF
Output Capacitance	C_{out}		—	9	11	pF

■ TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION



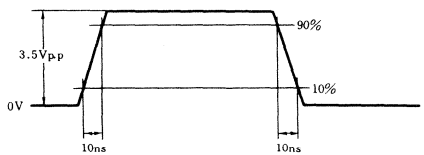
Load A



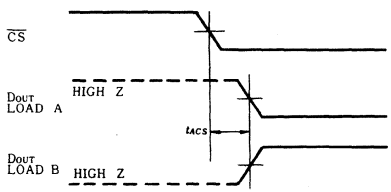
Load B

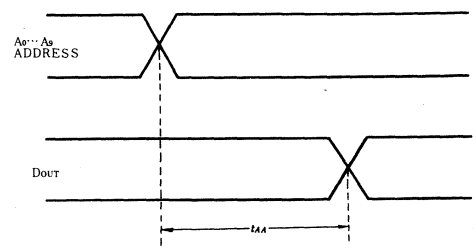
Note: C_L includes probe and stray capacitance

2. INPUT PULSE



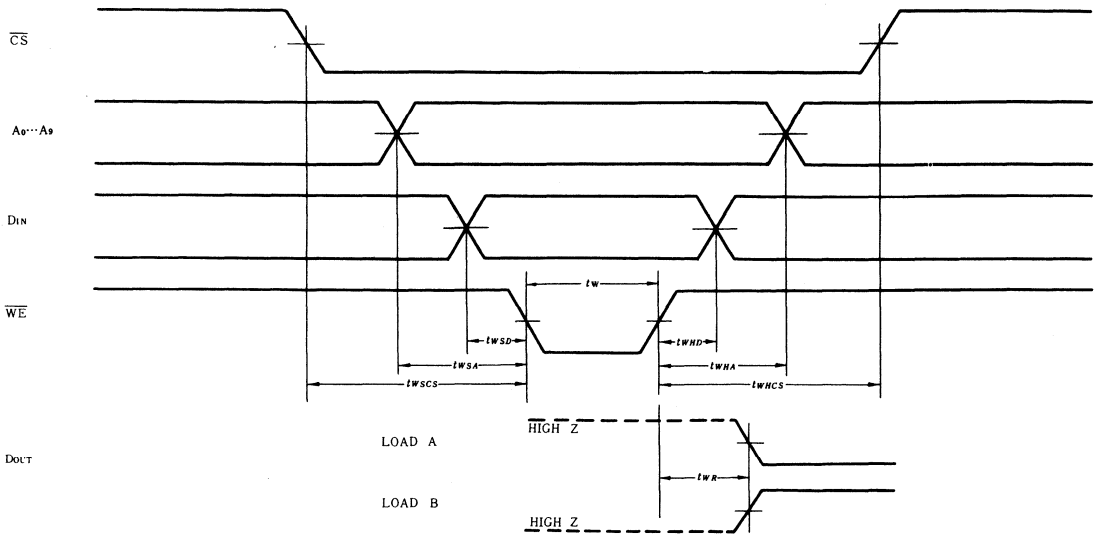
3. READ MODE





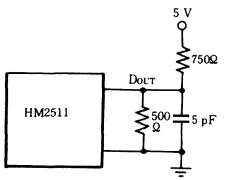
(All time measurements refer to 1.5V)

4. WRITE MODE

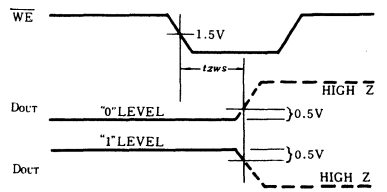


(All above measurements referenced to 1.5V)

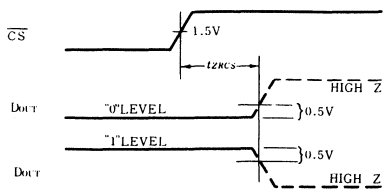
5. WRITE ENABLE TO HIGH Z DELAY



Load C



6. PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



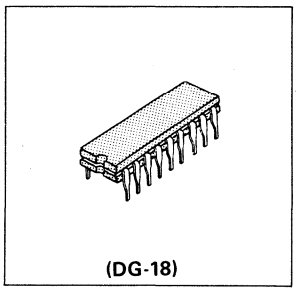
(All tZXXX parameters are measured at a delta of 0.5V from the logic level and using Load C.)

BIPOLAR PROM

HN25044, HN25045

1024-word x 4-bit Programmable Read Only Memory

The HITACHI HN25044 and HN25045 are high speed electrically programmable, fully decoded TTL Bipolar 4096 bit read only memories organized at 1024 words by 4 bits with on-chip address decoding and two chip enable inputs. The HN25044 and HN25045 are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

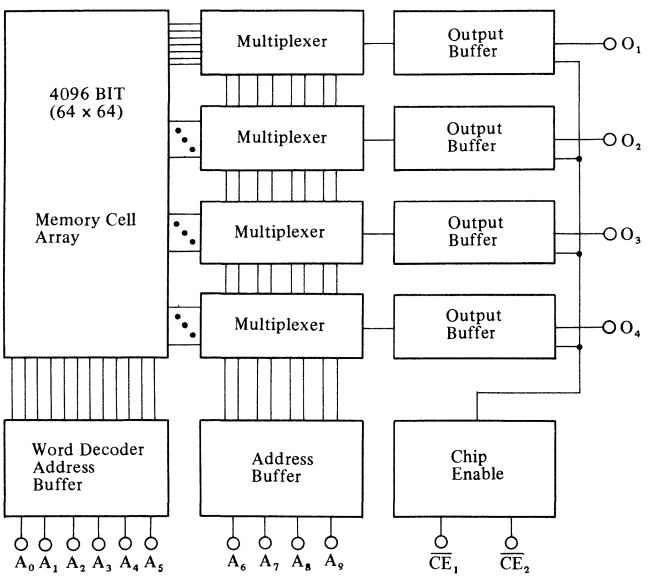


(DG-18)

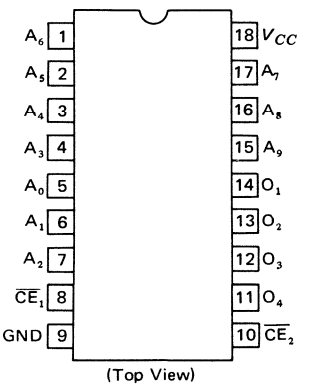
■ FEATURES

- 1024 words x 4 bits organization (fully decoded)
- DTL/TTL Compatible inputs and outputs
- Fast read access time; 35 ns typ. (50 ns max.)
- Medium power consumption; 500 mW typ.
- Two Chip enable inputs for memory expansion
- Open collector outputs (HN25044)/Three-state outputs (HN25045)
- Standard cerdip 18-pin package

■ BLOCK DIAGRAM

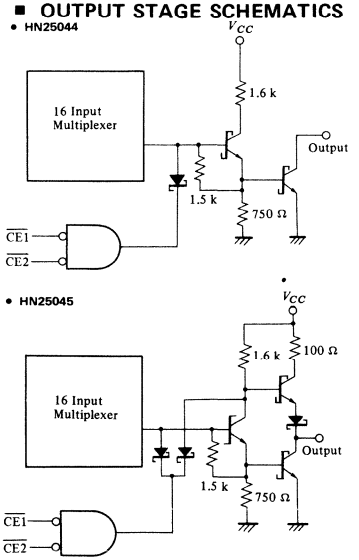


■ PIN ARRANGEMENT



(Top View)

■ OUTPUT STAGE SCHEMATICS



■ ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to +5.5	V
Output Voltage	V_{OUT}	−0.5 to +5.5	V
Output Current	I_{OUT}	50	mA
Operating Temperature	T_{opr}	−25 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

■ DC CHARACTERISTICS (V_{CC}=4.75 to 5.25 V, T_a=0 to +75°C)

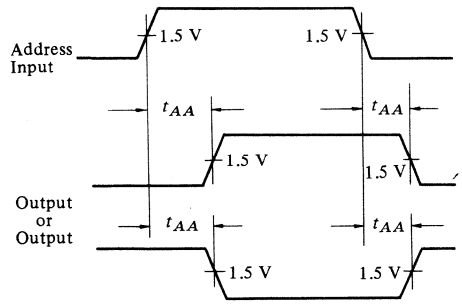
Item	Symbol	Test Condition	HN25044			HN25045			Unit
			min.	typ.	max.	min.	typ.	max.	
Input Voltage	V_{IH}		2.0	–	–	2.0	–	–	V
	V_{IL}		–	–	0.8	–	–	0.8	V
Output Voltage	V_{OH}	I_{OH}=–2 mA	–	–	–	2.4	–	–	V
	V_{OL}	I_{OL}=16 mA	–	–	0.45	–	–	0.45	V
Input Current	I_{IH}	V_{IH}=2.7 V	–	–	40	–	–	40	μA
	I_{IL}	V_{IL}=0.4 V	–	–	–0.4	–	–	–0.4	mA
Output Leakage Current	I_{OLK}	V_{out}=5.5 V	–	–	100	–	–	100	μA
		V_{out}=0.4 V	–	–	40	–	–	40	
Input Clamp Voltage	V_I	I_{in}=–18 mA	–	–	–1.2	–	–	–1.2	V
Power Supply Current	I_{CC}	Input Either Open or at Ground	–	100	130	–	100	130	mA
Output Short-circuit Current	I_{OS}	V_{out}=0 V	–	–	–	15	30	60	mA
Input Capacitance	C_{in}	V_{in}=2 V, V_{CC}=0 V	–	5	10	–	5	10	pF
Output Capacitance	C_{out}	V_{out}=0 V, V_{CC}=0 V	–	7	12	–	7	12	pF

■ AC CHARACTERISTICS (V_{CC}=4.75 to 5.25 V, T_a=0 to 75°C)

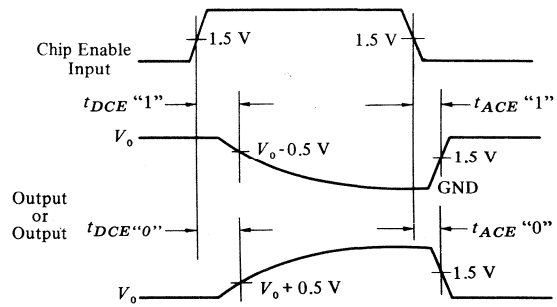
Item	Symbol	min.	typ.	max.	Unit
Address Access Time	t_{AA}	–	35	50	ns
Chip Enable Access Time	t_{ACE}	–	20	30	ns
Chip Enable Disable Time	t_{DCE}	–	20	30	ns

Notes: 1. Typ. value is at V_{CC}= 5.0 V and T_a= 25°C
2. Output disable time is the time taken for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5 V from the active output level.

■ SWITCHING WAVEFORMS

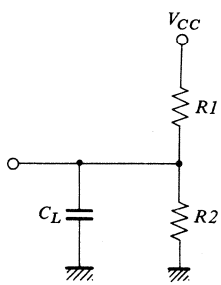


ACCESS TIME VIA ADDRESS INPUTS



OUTPUT ENABLE AND DISABLE TIMES

■ SWITCHING TIME TEST CONDITIONS



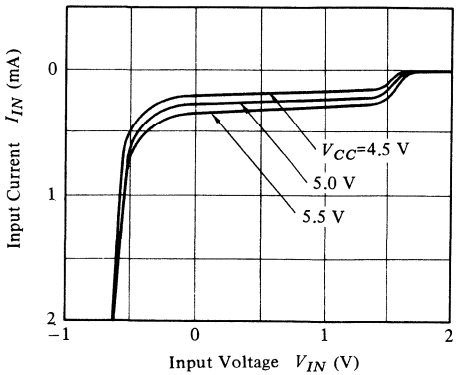
OUTPUT LOAD CIRCUIT

SWITCHING PARAMETER	HN25044			HN25045		
	R1	R2	C_L	R1	R2	C_L
t_{AA}	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF
t_{ACE} "1"	–	–	–	∞	600Ω	10 pF
t_{ACE} "0"	300Ω	600Ω	10 pF	300Ω	600Ω	10 pF
t_{DCE} "1"	–	–	–	∞	600Ω	30 pF
t_{DCE} "0"	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF

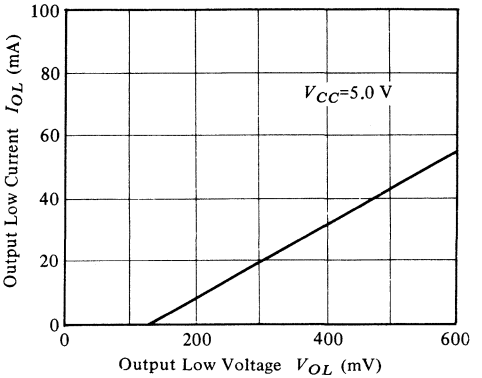
INPUT CONDITIONS
Amplitude – 0 V to 3 V
Rise and Fall time – 5ns from 1 V to 2 V
Frequency – 1 MHz

■ TYPICAL DC CHARACTERISTICS

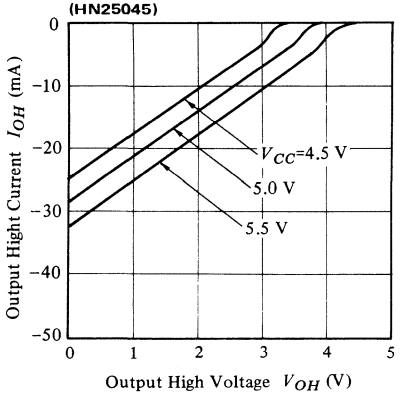
INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT LOW CURRENT VS. OUTPUT LOW VOLTAGE

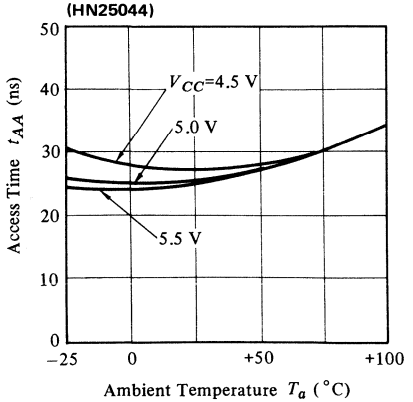


OUTPUT HIGH CURRENT VS. OUTPUT HIGH VOLTAGE (HN25045)

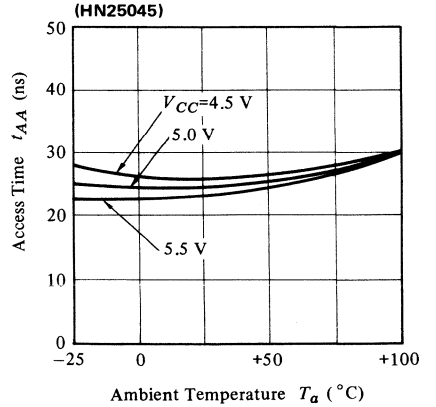


■ TYPICAL AC CHARACTERISTICS

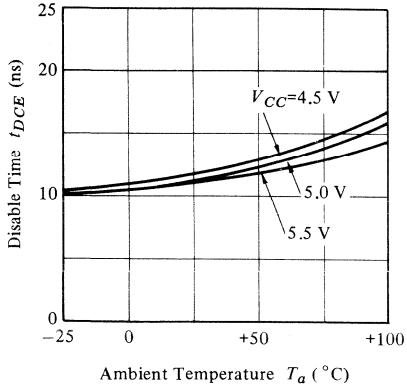
ACCESS TIME VS. AMBIENT TEMPERATURE (HN25044)



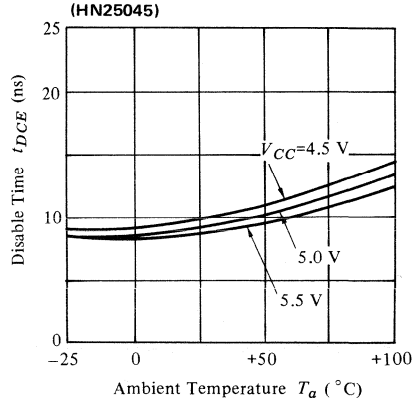
ACCESS TIME VS. AMBIENT TEMPERATURE (HN25045)



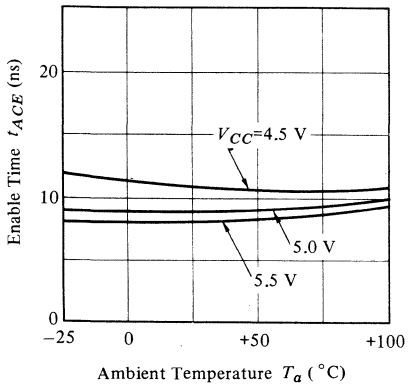
DISABLE TIME VS. AMBIENT TEMPERATURE (HN25044)



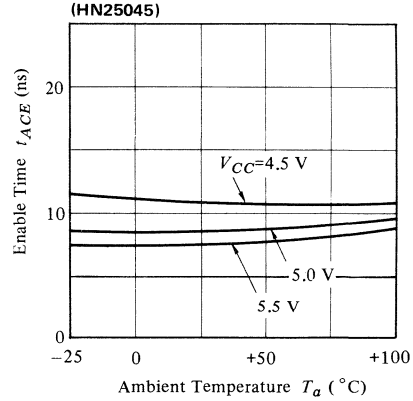
DISABLE TIME VS. AMBIENT TEMPERATURE (HN25045)



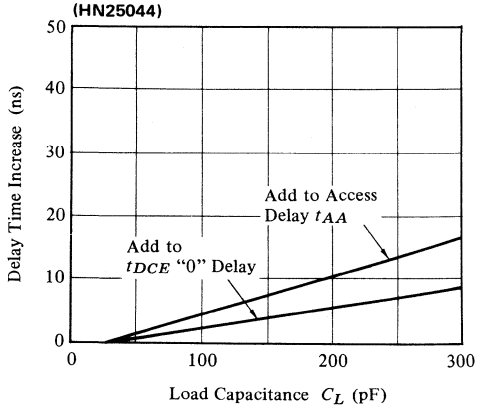
ENABLE TIME VS. AMBIENT TEMPERATURE (HN25044)



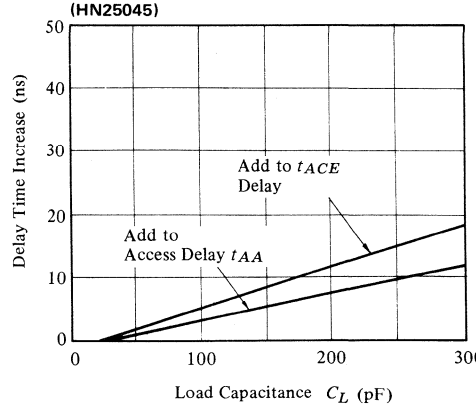
ENABLE TIME VS. AMBIENT TEMPERATURE (HN25045)



DELAY TIME INCREASE VS. LOAD CAPACITANCE (HN25044)



DELAY TIME INCREASE VS. LOAD CAPACITANCE (HN25045)



■ PROGRAMMING INFORMATION

Hitachi's sophisticated Fine Emitter technology and programming pulse method enables higher programmability and faster programming time ordinary PROMs, for the highest reliability.

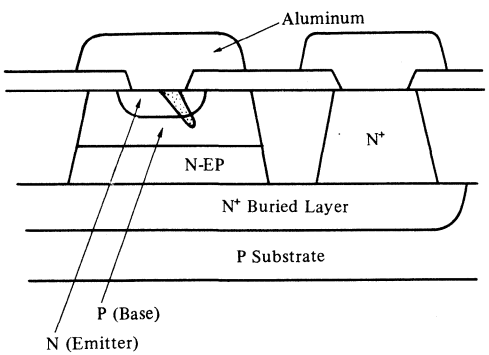
Fast programming time of typically 10 μs/bit is achieved with a fine emitter cell which requires less programming energy; thus, negligible thermal stress. Further, Hitachi advanced technology allows very high programmability of typically 99%.

To assure that the element is programmed properly, an additional four programming pulses are applied immediately after a sense pulse indicates conduction in the programmed bit. This high reliability feature virtually eliminates aluminum migration in the programmed cell.

One extra row and one extra column of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

The device is manufactured with outputs low (positive logic "zero") in all storage cells. To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

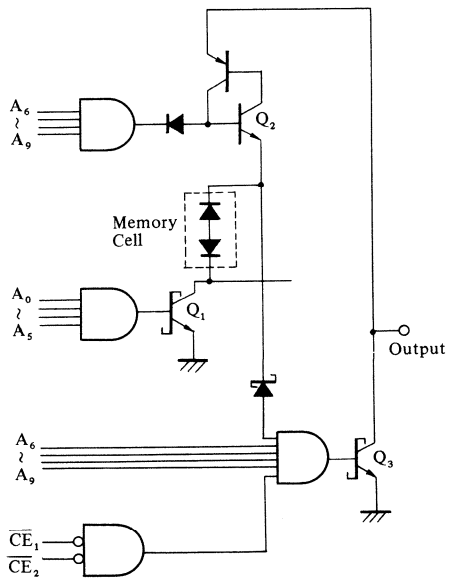
PROGRAMMED CELL (CROSS SECTION)



A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using eight address inputs to turn on transistors Q1 and Q2. By taking either (or both) chip enable inputs high, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through the junction into transistor Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the sensed voltage indicates that the selected bit is in the logic in state.

An additional 4 programming pulses are required to ensure that the bit is fully programmed, and to achieve high reliability. One output must be programmed at a time, since the internal decording circuit is capable of sinking only one unit of programming current at time.

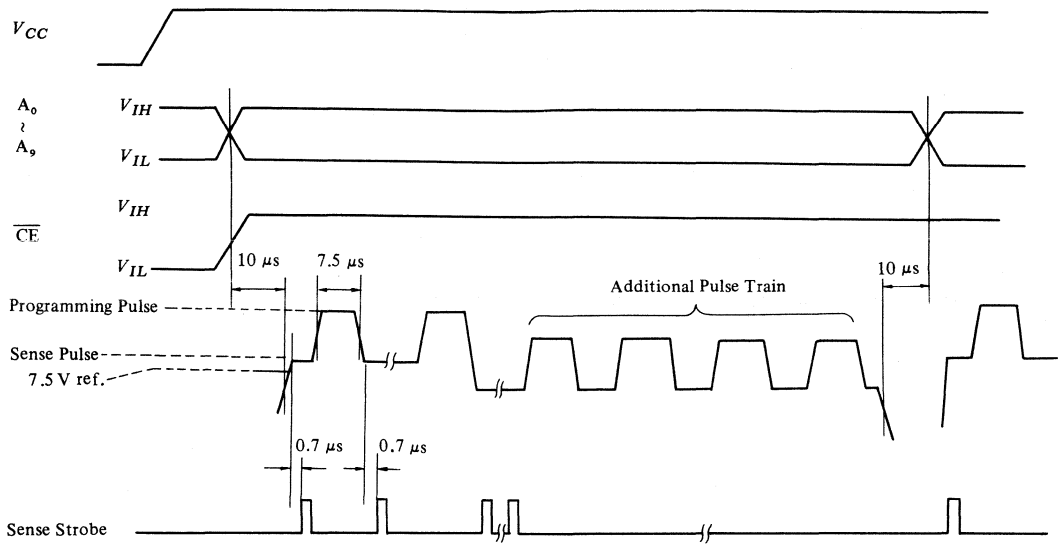
INTERNAL PROGRAMMING CIRCUIT



■ PROGRAMMING SPECIFICATION

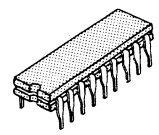
Characteristic	Limit	Unit	Notes
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	130 ± 5%	mA	
Clamp Voltage	20 + 0%-2%	V	
Ramp Rate	70 max.	V/μs	
Pulse Width	7.5 ± 5%	μs	10 V point/150Ω load
Duty Cycle	70% min.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	20 + 0%-2%	V	
Ramp Rate	70 max.	V/μs	
Sense current interruption before and after address change	10 min.	μs	
Programming V_{CC}	5.0 + 5%-0%	V	
Maximum Sensed Voltage for programmed "1"	7.5 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 min.	μs	
Programming Time Allocation/Bit	100 max.	ms	
Additional Programming Pulse Number	4	Time	

■ TYPICAL WAVEFORMS



2048-word×4-bit Programmable Read Only Memories

The HITACHI HN25084 and HN25085 are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 2048 word by 4 bit with on-chip address decoding and one chip enable input. The HN25084 and HN25085 are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

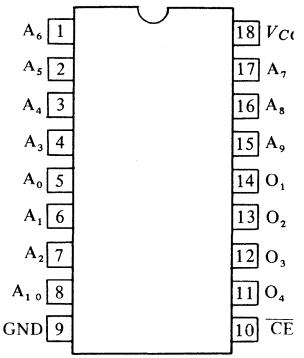


(DG-18)

■ FEATURES

- 2048 word x 4 bit organization (fully decoded)
- DTL/TTL compatible inputs and outputs
- Fast read access time: 40 ns typ. (60 ns max)
- Medium power consumption: 550 mW typ.
- One chip enable input for memory expansion
- Open collector outputs (HN25084)/Three-state outputs (HN25085)
- Standard cerdip 18-pin dual in-line package

■ PIN ARRANGEMENT



(Top View)

■ OPERATION

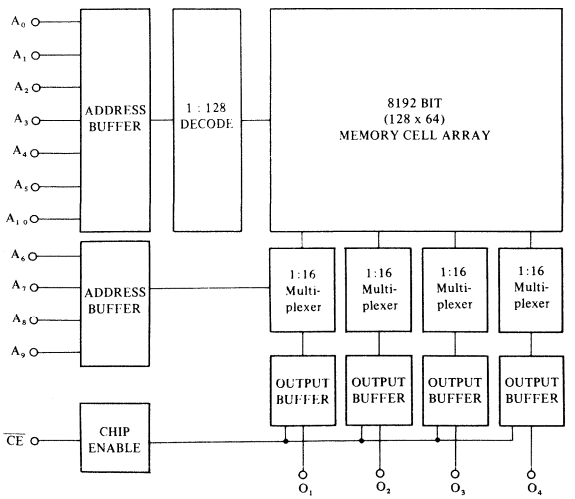
- **Programming**

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the eleven address inputs in TTL level. The device is disabled by bringing $\overline{CE}$ to a logic "one". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic "one" state, an additional pulse train is applied, then is stopped.

- **Reading**

To read the memory the device is enabled by bringing $\overline{CE}$ to a logic "zero". The outputs then correspond to the data programmed in the selected word.

■ LOGIC DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to +5.5	V
Output Voltage	V_{OUT}	−0.5 to +5.5	V
Output Current	I_{OUT}	50	mA
Operating Temperature	T_{opr}	−25 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

DC CHARACTERIESTICS (V_{CC} = 4.75 to 5.25 V, T_a = 0 to 75°C)

Characteristic	Symbol	Test Conditions	min.	typ.	max.	Unit
Input High Voltage	V_{IH}		2.0	–	–	V
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Current	I_{IH}	V_I = 2.7 V	–	–	40	μA
Input Low Current	$-I_{IL}$	V_I = 0.4 V	–	–	0.40	mA
Output Low Voltage	V_{OL}	I_O = 16 mA	–	–	0.45	V
Output Leakage Current	I_{OLK1}	V_O = 5.25 V	–	–	100	μA
Output Leakage Current	I_{OLK2}	V_O = 0.4 V	–	–	40	μA
Input Clamp Voltage	V_{IC}	I_I = −18 mA	–		−1.2	V
Power Supply Current	I_{CC}	Inputs Either Open or at Ground	–	110	150	mA
Output High Voltage*	V_{OH}	I_O = −2 mA	2.4	–	–	V
Output Short Circuit Current*	$-I_{OS}$	V_O = 0V	15	–	60	mA

* Note: Applicable to HN25089 only.

AC CHARACTERISTICS (V_{CC} = 4.75 to 5.25 V, T_a = 0 to 75°C)

Characteristic	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Access Time	t_{AA}		–	40	60	ns
Chip Enable Access Time	t_{ACE}		–	20	35	ns
Chip Enable Disable Time	t_{DCE}		–	20	35	ns

Note 1. Output Load: See Fig. 1.

Note 2. Measurement Reference: 1.5 V for both inputs and outputs.

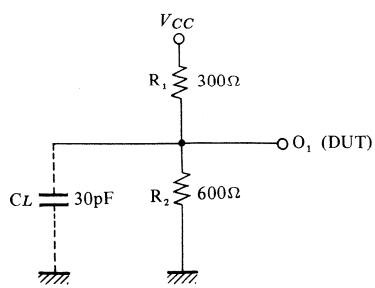
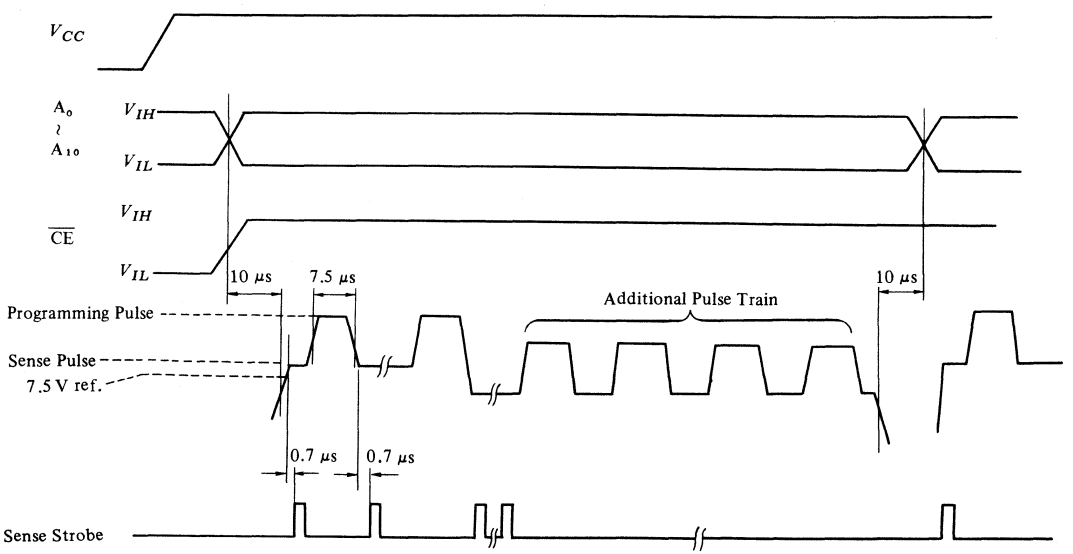


Fig. 1

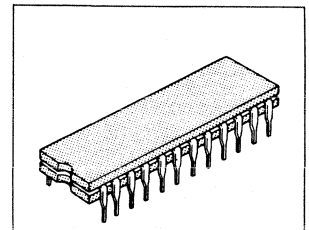
■ PROGRAMMING SPECIFICATION

Characteristic	Limit	Unit	Notes
Ambient Temperature	25±5	°C	
Programming Pulse			
Amplitude	130±5%	mA	
Clamp Voltage	20±2%	V	
Ramp Rate	70 max.	V/μs	
Pulse Width	7.5±5%	μs	10 V point/150Ω load
Duty Cycle	70% min.		
Sense Current			
Amplitude	20±0.5	mA	
Clamp Voltage	20±2%	V	
Ramp Rate	70 max.	V/μs	
Sense Current Interruption before and after address change	10 min.	μs	
Programming V_{CC}	5.0+5%−0%	V	
Maximum Sensed Voltage for programmed "1"	7.5±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 min.	μs	
Programming Pulse Number	100 max.	ms	
Additional Programming Pulse Number	4	Time	



1024-word × 8-bit Programmable Read Only Memories

The HITACHI HN25088 and HN25089 are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 1024 words by 8 bits with on-chip address decoding and four chip enable inputs. The HN25088 and HN25089 are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.



(DG-24)

■ FEATURES

- 1024 words x 8 bits organization (fully decoded)
- DTL/TTL compatible inputs and outputs
- Fast read access time: 40 ns typ. (60 ns max)
- Medium power consumption: 600 mW typ.
- Four chip enable inputs for memory expansion
- Open collector outputs (HN25088)/Three-state outputs (HN25089)
- Standard cerdip 24-pin dual in-line package

■ OPERATION

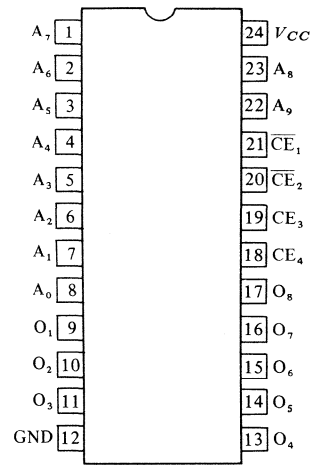
• Programming

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing $\overline{CE1}$ and/or $\overline{CE2}$ to as logic "one" or CE3 and/or CE4 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

• Reading

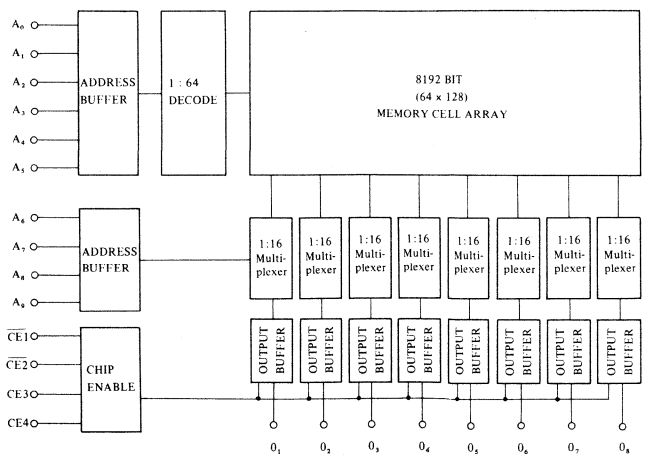
To read the memory the device is enabled by bringing $\overline{CE1}$ and $\overline{CE2}$ to a logic "zero", CE3 and CE4 to a logic "one". The outputs then corresponed to the data programmed in the selected word.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to +5.5	V
Output Voltage	V_{OUT}	−0.5 to +5.5	V
Output Current	I_{OUT}	50	mA
Operating Temperature	T_{opr}	−25 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

■ DC CHARACTERISTICS (V_{CC}=4.75 to 5.25 V, T_a=0 to +75°C)

Characteristic	Symbol	Test Conditions	min.	typ.	max.	Unit
Input High Voltage	V_{IH}		2.0	–	–	V
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Current	I_{IH}	V_I = 2.7 V	–	–	40	μA
Input Low Current	$-I_{IL}$	V_I = 0.4 V	–	–	0.40	mA
Output Low Voltage	V_{OL}	I_O = 16 mA	–	–	0.45	V
Output Leakage Current	I_{OLK1}	V_O = 5.25 V	–	–	100	μA
Output Leakage Current	I_{OLK2}	V_O = 0.4 V	–	–	40	μA
Input Clamp Voltage	V_{IC}	I_I = −18 mA	–	–	−1.2	V
Power Supply Current	I_{CC}	Inputs Either Open or at Ground	–	120	160	mA
Output High Voltage*	V_{OH}	I_O = −2 mA	2.4	–	–	V
Output Short Circuit Current*	$-I_{OS}$	V_O = 0 V	15	–	60	mA

* Note: Applicable to HN25089 only.

■ AC CHARACTERISTICS (V_{CC}= 4.75 to 5.25 V, T_a = 0 to 75°C)

Characteristic	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Access Time	t_{AA}		–	40	60	ns
Chip Enable Access Time	t_{ACE}		–	20	35	ns
Chip Enable Disable Time	t_{DCE}		–	20	35	ns

Note 1. Output Load: See Fig. 1.

Note 2. Measurement Reference: 1.5 V for both inputs and outputs.

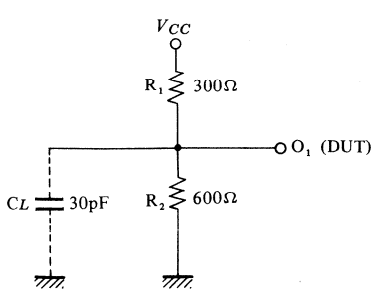
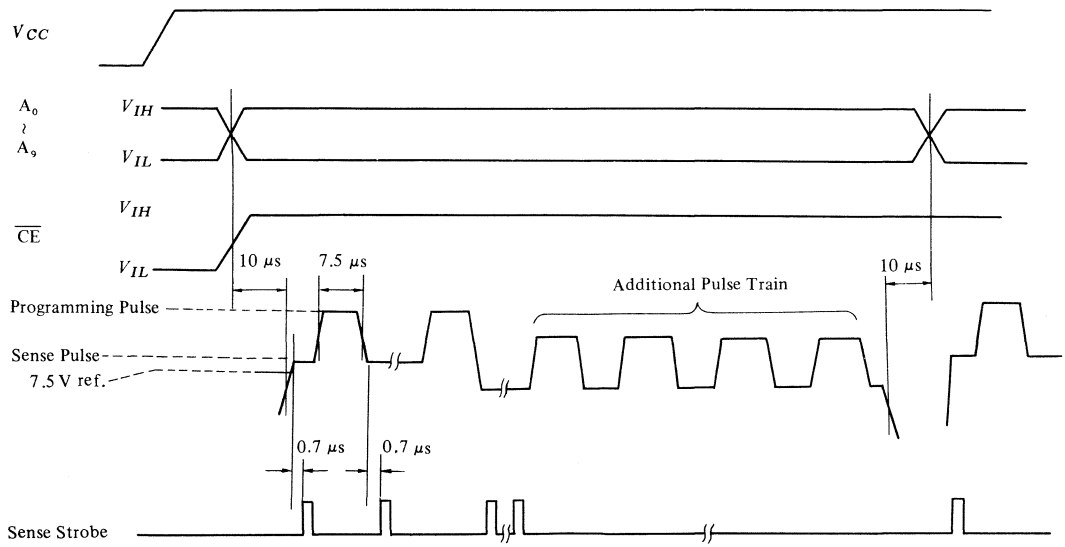


Fig. 1

PROGRAMMING SPECIFICATION

Characteristic	Limit	Unit	Notes
Ambient Temperature	25±5	°C	
Programming Pulse			
Amplitude	130±5%	mA	
Clamp Voltage	20±2%	V	
Ramp Rate	70 max.	V/μs	
Pulse Width	7.5±5%	μs	10 V point/150Ω load
Duty Cycle	70% min.		
Sense Current			
Amplitude	20±0.5	mA	
Clamp Voltage	20±2%	V	
Ramp Rate	70 max.	V/μs	
Sense Current Interruption before and after address change	10 min.	μs	
Programming V_{CC}	5.0+5%–0%	V	
Maximum Sensed Voltage for programmed "1"	7.5±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 min.	μs	
Programming Pulse Number	100 max.	ms	
Additional Programming Pulse Number	4	Time	



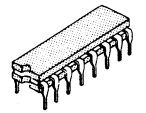
MEMORY SUPPORT CIRCUITS

HD2912

Quadruple TTL-to-MOS Clock Drivers

The HD2912, a clock driver for the MOS memory, has basically the NAND function. Its input is a TTL level and its output becomes an N MOS clock input level. It operates on two power supplies – V_{CC} (5V) and V_{DD} (12V). It anticipates taking as its load a maximum of ten units of 4K-bit N MOS memories and can drive a load capacity of 400 pF at high speed.

- TTL-MOS level converter circuit
- Switching time: 50 ns (max.)
- Load capacity drivable: 600pF
- Mounted with 4 circuits
- Applicable temperature: 0 to 70°C



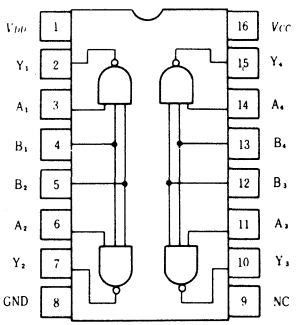
(DG-16)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HD2912	Unit
Supply Voltage	V_{CC} *	7.0	V
	V_{DD} *	18.0	V
Input Voltage	V_{in} *	5.5	V
Load Capacitance	C_L **	600	pF
Power Dissipation	P_T ***	800	mW
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* With respect GND
** per circuit
*** per package

■PIN ARRANGEMENT



(Top View)

■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{DD}	11.4	12	12.6	V
Operating Temperature	$Topr$	0	25	70	°C
Load Capacitance	C_L	100	—	600	pF
Damping Resistance	R_D	10	—	—	Ω

■ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{DD}=12V±5%)

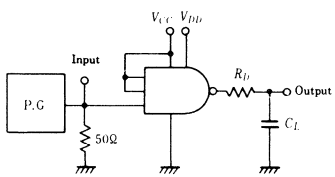
Item		Symbol	Test Condition	min.	typ. *	max.	Unit
Input Voltage		V_{IL}		2.0	—	—	V
		V_{IH}		—	—	0.8	V
Output Voltage		V_{OL}	V_{in}=2V, I_{OL}=0.1mA	—	0.45	0.6	V
		V_{OH}	V_{in}=0.8V, I_{OH}=−0.1mA	V_{DD}−0.9	11.5	—	V
Input Current	A	I_{IL}	V_{in}=0.4V	—	−1	−1.6	mA
	B	I_{IL}		—	−2	−3.2	mA
	A	I_{IH}	V_{in}=2.4V	—	—	40	μA
	B	I_{IH}		—	—	80	μA
		I_I	V_{in}=5.5V	—	—	1	mA
Power Supply Current		I_{DDH}	V_{in}=0V	—	16	24	mA
		I_{DDL}	V_{in}=5V	—	—	0.5	mA
		I_{CCH}	V_{in}=0V	—	12	18	mA
		I_{CCL}	V_{in}=5V	—	67	100	mA
Input Clamp Voltage		V_I	I_{in}=−12mA	—	—	−1.5	V

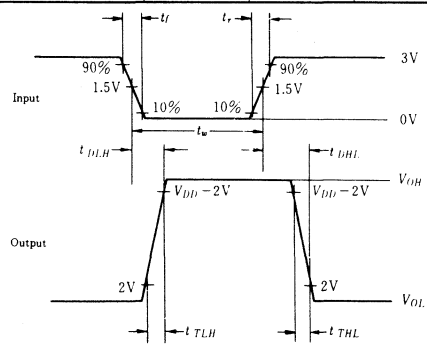
* V_{CC}=5V, V_{DD}=12V

■SWITCHING CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V, V_{DD}=12V)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Rising Delay Time	t_{DLH}	C_L=300pF R_D=0Ω	—	35	50	ns
Falling Delay Time	t_{DHL}		—	25	45	ns
Rise Time	t_{TLH}		—	12	25	ns
Fall Time	t_{THL}		—	12	25	ns

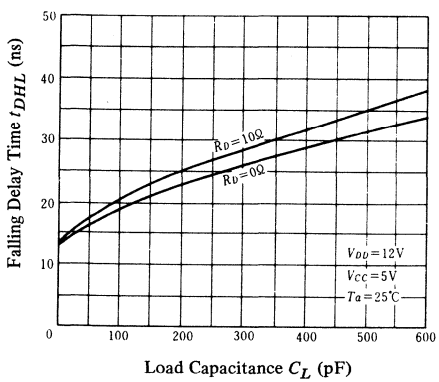
●TEST CIRCUIT AND WAVEFORMS



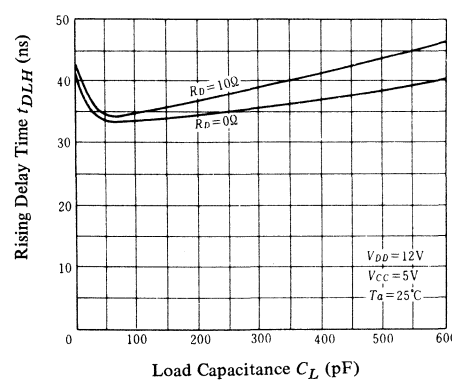


t_w=250ns, t_{cycle}=350ns, t_f = t_r = 10±1ns

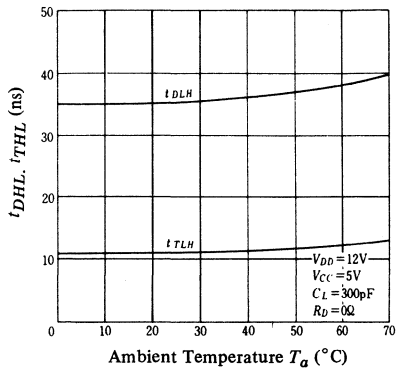
FALLING DELAY TIME vs. LOAD CAPACITANCE (1)



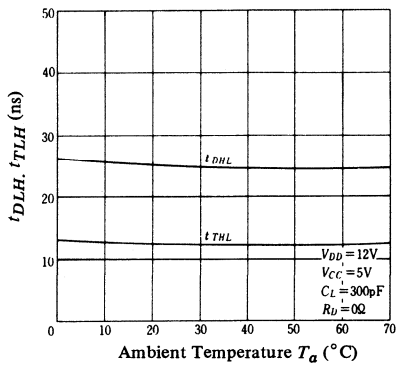
RISING DELAY TIME vs. LOAD CAPACITANCE (2)



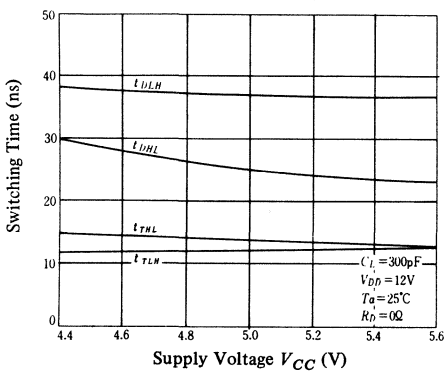
RISE TIME AND RISING DELAY TIME vs. AMBIENT TEMPERATURE



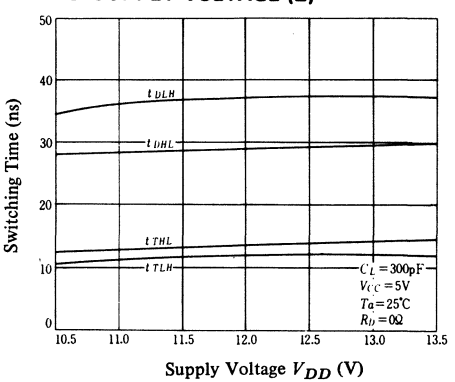
FALL TIME AND FALLING DELAY TIME vs. AMBIENT TEMPERATURE



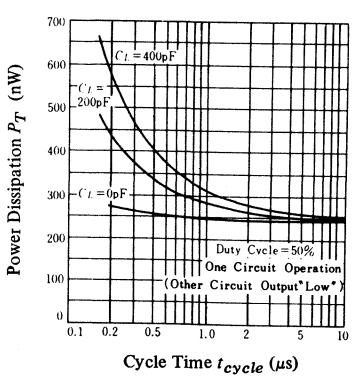
SWITCHING TIME vs. SUPPLY VOLTAGE (1)



SWITCHING TIME vs. SUPPLY VOLTAGE (2)



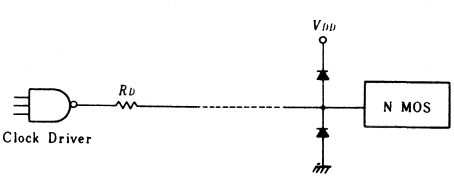
POWER DISSIPATION vs CYCLE TIME



■ ITEMS REQUIRING CARE WHEN USING THE HD2912

When measuring or mouting the HD2912, consider the following:

1. At the time of "H" level output, if a short circuit occurs between the output terminal and the other terminal (the GND terminal or input terminal), the element will break down.
2. When measuring the input/output characteristic of the circuit, do not place the input level in the vicinity of the threshold voltage (about 1.5V) for more than 10 seconds. If this caution is neglected, the element may break down.
3. If its load capacity is less than a certain value (100pF), sometimes this element cannot fully provide its function. Take note of this fact when designing a system.
4. When mounting this element, it is recommended providing the output terminal with a damping resistor (R_D) or a diode terminating circuit.

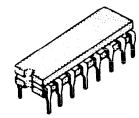


Quadruple TTL-to-NMOS Clock Drivers

The HD2916, a clock driver for the MOS memory, basically possesses a NAND function. Its input is a TTL level and its output becomes N MOS clock input level. It operates on two power supplies – V_{CC} (5V) and V_{DD} (12V). Assuming that a maximum of five units of 4K-bit NMOS memories may be connected, it is designed to drive a load capacity of 200pF at high speed.

FEATURES

- TTL-MOS level converter
- Switching time: 50 ns (max.)
- Average power consumption: 600mW (max.)
- Load capacity drivable: 300pF
- Mounted with 4 circuits
- Applicable temperature: 10 to 65°C



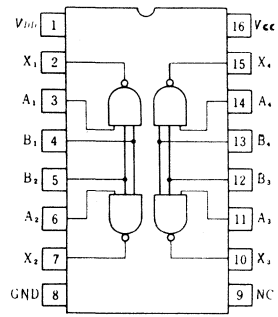
(DG-16A)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HD2916	Unit
Supply Voltage	V_{CC} *	−0.5 to+7	V
	V_{DD} *	−0.5 to+15	V
Input Terminal Voltage	V_{IN} *	−0.5 to+5.5	V
Output Load Capacitance	C_L **	300	pF
Power Dissipation	P_T ***	700	mW
Operating Temperature	T_{opr}	0 to+70	°C
Storage Temperature	T_{stg}	−50 to+150	°C

* With respect to GND
** Per circuit
*** Per package

PIN ARRANGEMENT



(Top View)

RECOMMENDED OPERATING CONDITION

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{DD}	11.4	12.0	12.6	V
Operating Temperature	$Topr$	10	25	55	°C
Input Voltage Level	V_{IH}	2.0	—	5.5	V
	V_{IL}	−0.5	—	0.8	V

■ELECTRICAL CHARACTERISTICS (Ta=10 to 55°C, V_{CC}=5V±5%, V_{DD}=12V±5%)

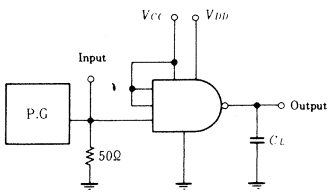
Item		Symbol	Test Condition	min.	typ. *	max.	Unit
Input Current	A	I_{IH}	V_{IN}=2.4V	—	—	40	μA
		I_{IL}	V_{IN}=0.4V	—	−1	−2	mA
	B	I_{IH}	V_{IN}=2.4V	—	—	80	μA
		I_{IL}	V_{IN}=0.4V	—	−2	−4	mA
Output Voltage		V_{OH}	V_{IN}=0.8V, I_{OH}=−50μA	V_{DD}−0.7	V_{DD}−0.4	—	V
		V_{OL}	V_{IN}=2.0V, I_{OL}=50μA	—	0.3	0.45	V
Supply Current		I_{DDH}	V_{IN}=0V	—	13	20	mA
		I_{CCH}	V_{IN}=0V	—	13	40	mA
		I_{DDL}	V_{IN}=5V	—	—	39	mA
		I_{CCL}	V_{IN}=5V	—	40	60	mA
Average Power Dissipation		P_{TA}	C_L=300pF, f=1MHz t_w=0.5μs, one circuit operation	—	300	600	mW

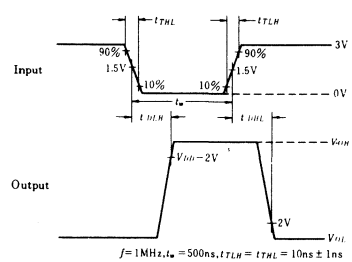
* V_{CC}=5V, V_{DD}=12V

■SWITCHING CHARACTERISTICS (Ta=10 to 55°C, V_{CC}=5V±5%, V_{DD}=12V±5%)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Output Delay Time	t_{DLH}	C_L=200pF f=1MHz t_{w_r}=0.5μs	—	—	50	ns
	t_{DHL}		—	—	50	ns

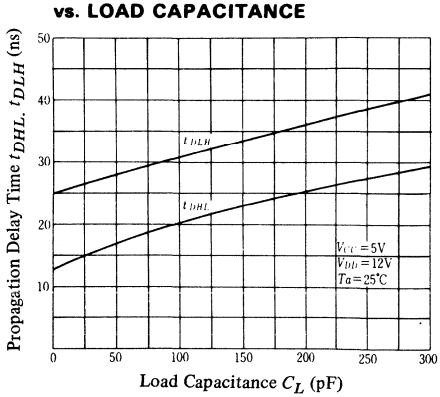
●TEST CIRCUIT & WAVEFORMS



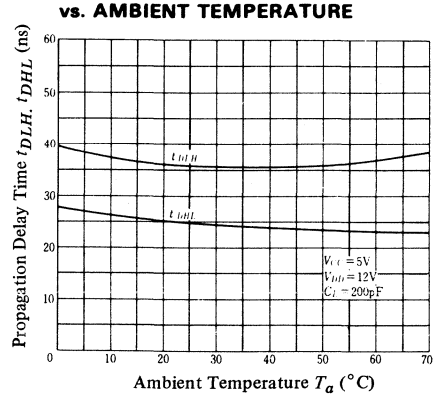


f=1MHz, t_w=500ns, t_{TLH}=t_{THL}=10ns±1ns

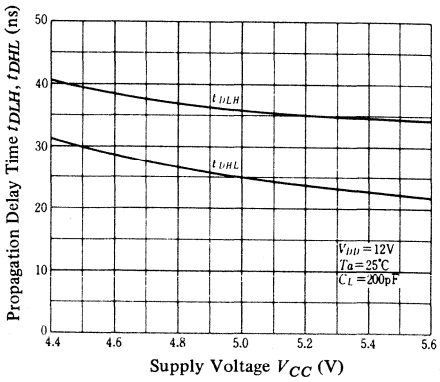
PROPAGATION DELAY TIME vs. LOAD CAPACITANCE



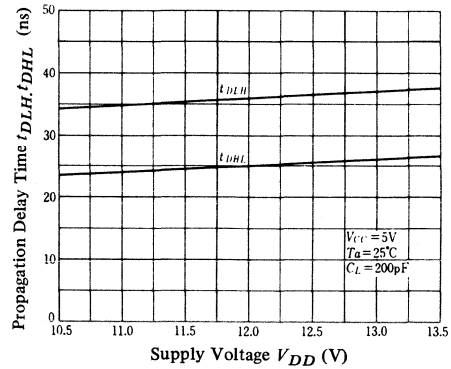
PROPAGATION DELAY TIME vs. AMBIENT TEMPERATURE



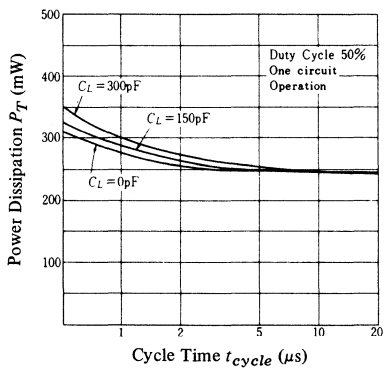
PROPAGATION DELAY TIME vs. SUPPLY VOLTAGE



PROPAGATION DELAY TIME vs. SUPPLY VOLTAGE



POWER DISSIPATION vs. CYCLE TIME



■ ITEMS REQUIRING CARE WHEN USING THE HD2916

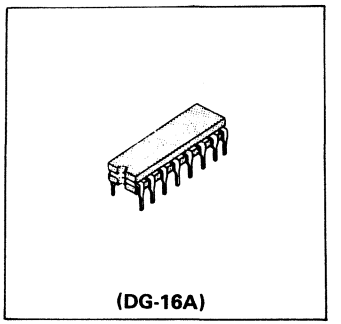
When measuring or mounting the HD2916, consider the following:

1. At the time of "H" level output, if a short circuit occurs between the output terminal and the other terminal (the GND terminal or input terminal), the element will break down.
2. When measuring the input/output characteristic of the circuit, do not place the input level in the vicinity of the threshold voltage (about 1.5V) for more than 10 seconds. If this caution is neglected, the element may break down.

HD2923

Quadruple ECL to TTL Drivers

The HD2923 is a monolithic, high speed Quadruple ECL to TTL Driver which accepts ECL input signals. It provides high output current suitable for driving the TTL clock inputs or other address multiplexing inputs of N-channel MOS memories such as the HM4816 or MK4116. Power supply requirements are ground, +5.0 Volts and −5.2 Volts. The HD2923 requires no paticular power supply sequencing in order to assure standby mode of memories, because the outputs are always "high" at applying the power. Propagation delay is 10ns MAX.
The HD2923 is fabricated by means of HITACHI's Schottky Bipolar technology to assure high performance over the 0°C to 75°C ambient temperature range.

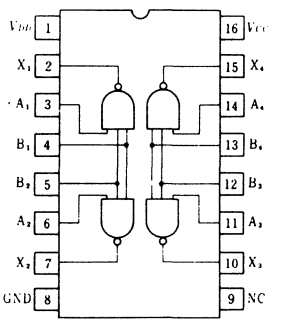


(DG-16A)

■ FEATURES

- High Speed
  t_{pd} = 10ns MAX. (50% to 2.2Vdc out or to +1.0Vdc out, 200pF Load)
- Low Power . . . . . 250mW typ. (DC)
- 10K ECL Compatible Inputs
- Pin Compatibility . . . . . MC10125 or HD10125

■ PIN ARRANGEMENT



(Top View)

The V_{BB} reference voltage is available on pin 1 for use in single ended input biasing.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
	V_{EE}	−7 to +0.5	V
Input Voltage	V_{IN}	V_{EE} to +0.5	V
Output Voltage	V_{OUT}	−1.0 to V_{CC} +1	V
Power Dissipation	P_T	1.0	W
Operating Temperature*	T_{opr}	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

*under bias

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{EE}	−5.46	−5.2	−4.94	V
Input Voltage	V_{IH}	−1.025	—	—	V
	V_{IL}	—	—	−1.520	V
Operating Temperature	T_{opr}	0	—	75	°C

■ TRUTH TABLE

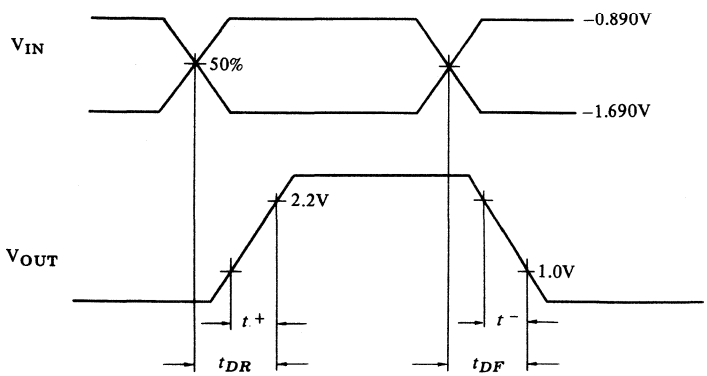
Input		Output
A	B	Y
H	V_{BB}	L
L	V_{BB}	H
H	L	L
L	H	H
V_{BB}	H	H
V_{BB}	L	L
Open	Open	H

■ DC CHARACTERISTICS

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Power Supply Drain Current	$-I_{EE}$	$V_{EE}=-5.2V$, $V_{CC}=5.0V$	—	22	27	mA
	I_{CCH}		—	23.5	29	mA
	I_{CCL}		—	34.5	42	mA
Input Current	I_{inH}	$V_{IN}=-0.81V$	—	—	115	μA
Input Leakage Current	I_{CBO}	$V_{IN}=-5.2V$	—	—	1.0	μA
Output Voltage	V_{OH}	$I_{OH}=-1.0mA$	2.7	—	—	V
	V_{OL}	$I_{OL}=5.0mA$	—	—	0.5	V
Threshold Voltage	V_{OHA}	$V_{IH}=-1.1V$, $I_{OH}=-1.0mA$	2.7	—	—	V
	V_{OLA}	$V_{IL}=-1.48V$, $I_{OL}=5.0mA$	—	—	0.5	V
Indeterminate Input Protection Tests	V_{OHS}	All inputs = V_{EE}	2.7	—	—	V
		All inputs = Open	2.7	—	—	
Reference Voltage	V_{BB}		−1.420	—	−1.150	V
Common Mode Rejection Tests	V_{OHC}	$V_{INH}=0.300V$, $V_{INL}=-0.825V$	2.7	—	—	V
		$V_{INH}=-1.890V$, $V_{INL}=-2.890V$	2.7	—	—	
	V_{OLC}	$V_{INH}=0.300V$, $V_{INL}=-0.825V$	—	—	0.5	V
		$V_{INH}=-1.890V$, $V_{INL}=-2.890V$	—	—	0.5	

■ AC CHARACTERISTICS

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Propagation Delay Time	t_{DR}	50% to +2.2V, $C_L=200pF$	—	—	10	ns
	t_{DF}	50% to +1.0V, $C_L=200pF$	—	—	10	ns
Rise Time	t^+	+1.0V to +2.2V, $C_L=200pF$	—	—	5	ns
Fall Time	t^-	+2.2V to +1.0V, $C_L=200pF$	—	—	5	ns



CROSS-REFERENCE

Note)

HM472114-3	
300	P, G

- HM472114-3 — Type No.
- P, G — Package Material
- 300 — Access Time (ns) max

1. MOS RAM

Mode	Structure	Total Bit	Organization	Number of Pin	Hitachi	Intel
Dynamic	NMOS	16k	16384 x 1	16		2117-5
						300 P, G
					HM4716A-4	2117-4
					250 P, G	250 P, G
					HM4716A-3	2117-3
					200 P, G	200 P, G
					HM4716A-2	2117-2
					150 P, G	150 P, G
					HM4716A-1	
					120 P, G	
					HM4816	
					100 C	
		64k	65536 x 1	16		
					HM4864-2	
					150 C	
					HM4864-3	
					200 C	
Static	NMOS	4k	1024 x 4	18	HM472114A	
					150 P, G	
					HM472114A-2	2114/L-2
					200 P, G	200 P, G
					HM472114-3	2114/L-3
					300 P, G	300 P, G
					HM472114-4	2114/L
					450 P, G	450 P, G
						2148-3
						55 G
					(HM6148)	2148
					70 P	70 G

Texas		Mostek		Motorola		NEC		Toshiba		Mitsubishi		Fujitsu	
				MCM4116-30		μPD416							
				300	G, C	300	P, G						
TMS4116-25		MK4116-4		MCM4116-25		μPD416-1		TMM416-4		M5K4116-4		MB8116N	
250	P, G, C	250	P, G	250	G, C	250	P, G	250	G	250	P, G	250	C
TMS4116-20		MK4116-3		MCM4116-20		μPD416-2		TMM416-3		M5K4116-3		MB8116E	
200	P, G, C	200	P, G	200	G, C	200	P, G	200	G	200	P, G	200	C
TMS4116-15		MK4116-2		MCM4116-15		μPD416-3		TMM416-2		M5K4116-2		MB8116H	
150	P, G, C	150	P, G	150	G, C	150	P, G	150	G	150	P, G	150	C
												MB8216E	
												120	C
		MK4164-10											
		100	C										
		MK4164-12								M58764-12			
		120	C							120	C		
TMS4164-15				MCM6664-15						M58764-15			
150	C			150	C					150	C		
				MCM6664-20									
				200	C								
												MB8164H	
												120	C
												MB8164E	
												200	C
												MB8164N	
												250	C
TMS4045-15						μPD2114L-5						MB8114H	
150	P, G, C					150	P, G					150	P, C
TMS40/L45-20		MK4114-3		MCM21/L14-20		μPD2114L-3		TMM314A/L1		M5L2114L-2		MB8114EL	
200	P, G, C	200	P, C	200	P, C	200	P, G	200	P	200	P, G	200	P, C
TMS40/L45-25		MK4114-4		MCM21/L14-25		μPD2114L-2							
250	P, G, C	250	P, C	250	P, C	250	P, G						
		MK4114-5		MCM21/L14-30		μPD2114L-1				M5L2114L-3		MB8114NL	
		300	P, C	300	P, C	300	P, G			300	P, G	300	P, C
TMS40/L45-45				MCM21/L14-30		μPD2114		TMM314A/L		M5L2114L			
450	P, G, C			450	P, C	450	P, G	450	P	450	P, G		

Mode	Structure	Total Bit	Organization	Number of Pin	Hitachi	Intel
Static	CMOS	4k	4096 x 1	18	HM6147/L-3 55 P, G	
					HM6147/L 70 P, G	
					HM4315 450 P	
			1024 x 4	18	HM6148/L 70 P	
					HM6148/L-6 85 P	
					HM4334-3 300 P	
					HM4334-4 450 P	
		16k	2048 x 8	24	HM6116/L-2 120 P	
					HM6116/L-3 150 P	
					HM6116/L-4 200 P	

Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
						MB8404E
						250 G
		MCM146504		TC5504-1		
		450 P, C		550 P		
				TC5504-2		
				800 P		
			μPD444-3			
			200 P			
			μPD444-2			MB8414E
			250 P			250 G
			μPD444-1			
			300 P			
			μPD444		M58981-45	
			450 P		450 G	
				TC5514-1		
				650 P		
				TC5515-2		
				800 P		
				TC5516		
				250 P		

2. MOS ROM

Program	Structure	Total Bit	Organization	Number of Pin	Hitachi	Intel
Mask	NMOS	16k	2048 x 8	24	HN462316E 450 P	2316E 450 P, G
		32k	4096 x 8	24	HN46332 350 P	2332A 450 P, G
		64k	8192 x 8	24	HN48364 350 P	
				28		2364A 450 P, G
Electrically & UV Erasable	NMOS	16k	2048 x 8	24	HN462716 450 C, G	2716-1 350 C 2716-2 390 C 2716 450 C
		32k	4096 x 8	24	HN462732 450 C HN462532 450 C	2732 450 C

Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
	MK34000-3	MCM68A 316E		TMM334		MB8316
	350 P, C	350 P, C		450 P		450 P
	MK31000-3	MCM68A 316A	μPD2316	TMM331A	M58731	
	550 P, C	350 P, C	450 P, G	450 P	650 P, G	
			μPD2332	TMM333	M58333	MB8332
			450 P, G	450 P	650 P	200 P
TMS4732	MK32000-5	MCM68A 332				
450 P, G	300 P, G	350 P, C				
	MK36000-5	MCM68B 364				
	300 P, G	250 P, C				
		MCM68A 364			M58334	
		350 P, C			650 P	
			μPD2364	TMM2364		
			450 P, G	250 P		
	MK2716-6	MCM27A 16				
	350 C	350 C				
	MK2716-7					
	400 C					
	MK2716-8	MCM2716	μPD2716	TMM323	M5L2716	MB8516
	450 C	450 C	450 C	450 C	450 C	450 C
					M5L2716-65	
					650 C	
TMS2516						
450 G, C						
					M5L2732	MB8532
					450 C	450 C
					M5L2732-6	
					550 C	
TMS2532						
450 G, C						

3. Bipolar RAM

Structure	Total Bit	Organization	Number of Pin	Output	Hitachi		Fairchild	
TTL	256	256 x 1	16	O/C	HM2504-1		93411A	
					45	G	45	G
					HM2504		93411	
					55	G	55	G, F
	1k	1024 x 1	16	O/C	HM2510-2		93415A	
					35	G	35	G, F
					HM2510-1		93415	
					45	G	45	P, G, F
					HM2510			
					70	G		
				3-S			93425A	
							30	G, F
					HM2511-1		93425	
					45	G	45	G, F
					HM2511			
					70	G		
ECL	256	256 x 1	16		HM2105		F10410	
					35	G	30	P, G, F
					HM2106		F10411	
					15	G	35	P, G, F
					HM10414-1			
					8	G		
					HM10414		F10414	
					10	G	10	G, F
	1k	1024 x 1	16		HM2110-2		F10415A	
					20	G	20	G, F
					HM2110-1			
					25	G		
					HM2110		F10415	
					35	G	35	G, F
		256 x 4	24		HM10422		F10422	
					10	G	10	G, F
					HM100422		F100422	
					10	G	10	G, F
	4k	4096 x 1	18		HM10470		F10470	
					25	G	30	G
					HM10470-1			
					15	G		

Texas	Intel	Motorola	MMI	Signetics	NEC	Fujitsu
	3107A			N82S117		
	60 G, C			40 G		
SN74S301	3107		6530	74S301	μPB2206	
65 P, G	80 G, C		55 C	50 G	50 G	
				N93415A		
				35 G		
		MCM93415		N93415	μPB2205	MBM93415
		45 P, G, F		45 G	50 G	45 G
SN74S314A						
70 P, G						
				N93425A		
				35 G		
		MCM93425		N93425		
		45 G, F		45 G		
SN74S214A						
70 P, G						
SN10144		MCM10144			μPB10144	MBM10410
30 G, F		30 G, F			25 G	35 G
		MCM10152				MB7042
		45 G, F				14 G
						MBM10415AH
						20 C
		MCM10146				MBM10415A
		30 G, F				35 C
						MB7071H
						10 F

4. Bipolar PROM

Structure	Total Bit	Organization	Number of Pin	Output	Hitachi		Fairchild	
TTL	4k	1024 x 4	18	O/C				
					HN25044		93452	
					50	G	55	P, G
				3-S				
					HN25045		93453	
					50	G	55	P, G
	8k	2048 x 4	18	O/C	HN25084			
					60	G		
				3-S	HN25085			
					60	G		
		1024 x 8	24	O/C	HN25088		93451	
					60	G	45	P, G, F
				3-S	HN25089		93450	
					60	G	45	P, G, F

Texas		Intel		Motorola		MMI		Signetics		NEC		Fujitsu	
SN74S477		3605A-1											
35	P, G	50	G										
		3605A-2		MCM7642		6352-1		N82S136		μPB406		MB7059	
		60	G	70	G	60	G	60	G	70	G	70	G
SN74S476		3625A-1											
35	P, G	50	G										
		3625A-2		MCM7643		6353-1		N82S137		μPB426		MB7054	
		60	G	70	G	60	G	60	G	70	G	70	G
				MCM7684				N82S184					
				80	G			100	G				
				MCM7685				N82S185					
				80	G			100	G				
SN74S451		3608		MCM7680		6380-1		N82S180		μPB408		MB7060	
45typ	P, G	80	G	70	G	90	G	70	G	85	G	250	G
SN74S450		3628		MCM7681		6381-1		N82S181		μPB428		MB7055	
45typ	P, G	80	G	70	G	90	G	70	G	85	G	250	G

MEMO